Calculation of FM and AM Noise Signals of Colpitts Oscillators in the Time Domain

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Introduction

An oscillator is a combination of an amplifier, a resonator and phase modulator in a feedback loop. The value of the loop gain and its phase needs to be enough to start oscillation and after the steady state condition maintains oscillation. This is achieved either by voltage or current limiting, by AGC or limiting diodes and is well explained in [1], probably the best explanation of its kind. If such amplitude stabilization would not exist, the amplifier-oscillator would self-destruct. The limiting part of the oscillator keeps the AM (noise) well below the FM noise close-in, but very far-off they reach the same amplitude. Any deviation from this is due to a heavy unwanted non-linearity.

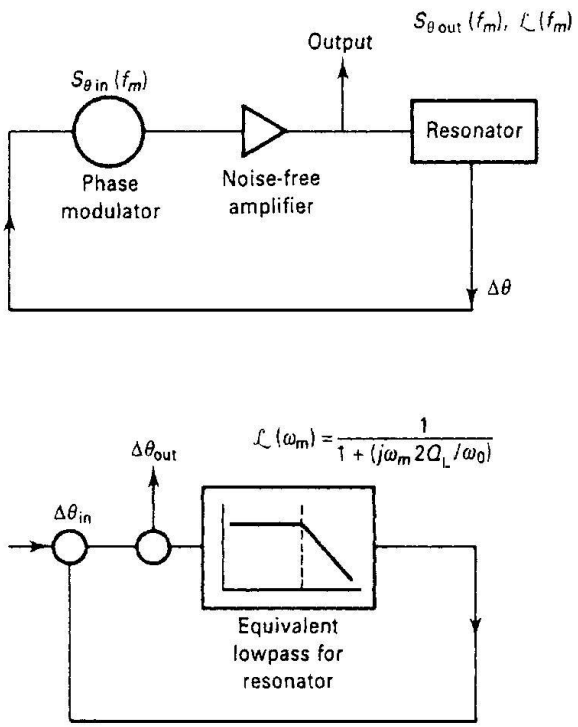

Figure 1 — Block diagram of oscillator and its low pass equivalent based on Leeson's model.

The topic here is to look at the noise of an oscillator.

The oscillator is under large signal condition and also acts like a mixer. Figure 1 shows the block diagram and its low pass equivalent based on Leeson's model [2]. The loop requirement was first mentioned in the Barkhausen analysis [3]. Initial open loop gain for getting started needs to be 3, because the steady state value is approximately 1/3 of the dc transconductance.

The noise has various sources and the following will look at all the steps [4-7]. For the reason of accuracy the following is a very detailed but complete mathematical analysis.

At the end of this, there will be a set of measurements including details about the results.

In all systems, amplifiers and oscillators, conditions of saturation (specifically with memory effects), tend to amplify AM components.

Noise Generation in Oscillators

As shown above, the qualitative linearized picture of noise generation in oscillators is very well known. The physical effects of random fluctuations taking place in the circuit are different depending on their spectral allocation with respect to the carrier:

Noise components at low frequency deviations result in frequency modulation of the carrier through mean square frequency fluctuation proportional to the available noise power.

Noise components at high frequency deviations result in phase modulation of the carrier through mean square phase fluctuation proportional to the available noise power.

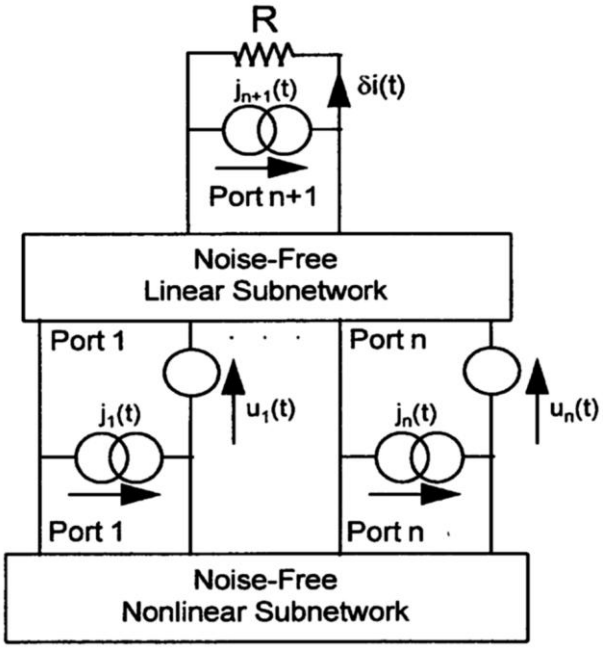

Figure 2 — Equivalent circuit of a general noisy nonlinear network

We will demonstrate that the same conclusions can be quantitatively derived from the HB equations for an autonomous circuit [5, 8].

Equivalent Representation of a Noisy Nonlinear Circuit

A general noisy nonlinear network can be described by the equivalent circuit shown in Figure 2. The circuit is divided into linear and nonlinear subnetworks as noise-free multi-ports. Noise generation is accounted for by connecting a set of noise voltage and noise current sources at the ports of the linear subnetwork [9-11].

Frequency Conversion Approach

The circuit supports a large-signal time periodic steady state of fundamental angular frequency ω_0 (carrier). Noise signals are small perturbations superimposed on the steady state, represented by families of pseudo-sinusoids located at the sidebands of the carrier harmonics. Therefore, the noise performance of the circuit is determined by the exchange of the power among the sidebands of the unperturbed steady state through frequency conversion in the nonlinear subnetwork. Due to the perturbative assumption, the nonlinear subnetwork can be replaced with a multi-frequency linear multi-port described by a conversion matrix. The flow of noise signals can be computed by means of conventional linear circuit techniques.

The frequency conversion approach frequently used has the following limitations:

The frequency conversion approach is not sufficient to predict the noise performance of an autonomous circuit. The spectral density of the output noise power, and consequently the PM noise computed by the conversion analysis are proportional to the available power of the noise sources.

- In the presence of both thermal and flicker noise sources, PM noise increases: as ω^{-1} for $\omega \to 0$; tends to a finite limit for $\omega \to \infty$.
- Frequency conversion analysis correctly predicts the far carrier noise behavior of an oscillator, and in particular the oscillator noise floor; does not provide results consistent with the physical observations at low deviations from the carrier.

This inconsistency can be removed by adding the modulation noise analysis. In order to determine the far away noise using the autonomous circuit perturbation analysis, the following applies.

The circuit supports a large-signal time-periodic autonomous regime. The circuit is perturbed by a set of small sources located at the carrier harmonics and at the sidebands at a deviation ω from carrier harmonics. The perturbation of the circuit state $(\delta \mathbf{X}_B, \delta \mathbf{X}_H)$ is given by the uncoupled sets of equations,

$$\left[\frac{\partial E_H}{\partial X_H}\right]_{ss} \partial X_H = J_H(\omega) \tag{1}$$

$$\left[\frac{\partial E_B}{\partial X_B}\right]_{ss} \partial X_B = J_B(\omega) \tag{2}$$

where,

E_B, E_H = vectors of HB errors

X_B, X_H = vectors of state variable (SV) harmonics (since the circuit is autonomous, one of the entries X is replaced by the fundamental frequency ω_0)

J_B, J_H = vectors of forcing terms

The subscripts B and H denote sidebands and carrier harmonics, respectively.

For a spot noise analysis at a frequency ω, the noise sources can be interpreted in either of two ways:

- Pseudo-sinusoids with random amplitude and phase located at the sidebands. Noise generation is described by Equation (1) which is essentially a frequency conversion equation relating the sideband harmonics of the state variables and of the noise sources. This description is exactly equivalent to the one provided by the frequency conversion approach. This mechanism is referred to as *conversion noise* [12-15].

Sinusoids located at the carrier harmonics are randomly phase-and-amplitude-modulated by pseudo-sinusoidal noise at frequency ω. Noise generation is described by Equation (2), which describes noise-induced jitter of the circuit-state, represented by the vector δX_H. The modulated perturbing signals are represented by replacing the entries of J_H with the complex modulation laws. This mechanism is referred to as *modulation noise*. One of the entries of δX_H is $\delta\omega_0$ where $\delta\omega_0(\omega)$ = phasor of the pseudo-sinusoidal components of the fundamental frequency fluctuations in a 1 Hz band at frequency ω. Equation (2) provides a frequency jitter with a mean square value proportional to the available noise power. In the presence of both thermal and flicker noise, PM noise raises as ω^{-3} for $\omega \to 0$ and tends to 0 for $\omega \to \infty$. Modulation noise analysis correctly describes the noise behavior of an oscillator at low deviations from the carrier and does not provide results consistent with physical observations at high deviations from the carrier.

The combination of both phenomena explains the noise in the oscillator shown in Figure 3, where the near carrier noise dominates below ω_X and far carrier noise dominates above ω_X.

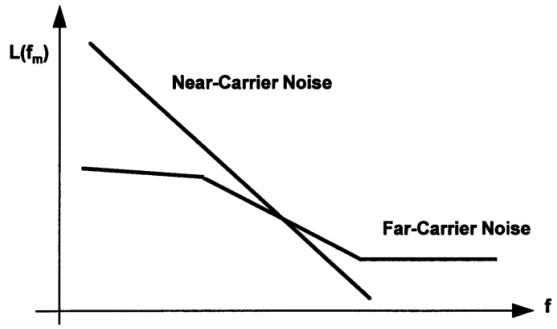

Figure 3 — Oscillator noise components.

Figure 4 (itemized form) shows the noise sources as they are applied at the IF. We have arbitrarily defined the low oscillator output as IF. This applies to the conversion matrix calculation.

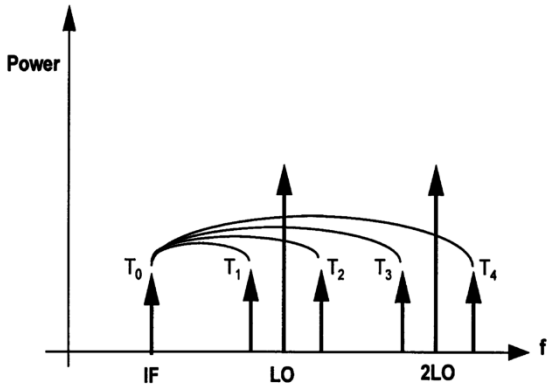

Figure 4 — Noise sources where the noise at each sideband contributes to the output noise at the IF through frequency conversion.

Figure 5 shows the total contributions which have to be taken into consideration for calculation of the noise at the output. The accuracy of the calculation of the phase noise depends highly on the quality of the parameter extraction for the nonlinear device; in particular, high frequency phenomena must be properly modeled. In addition, the flicker noise contribution is essential. This is also valid for mixer noise analysis.

Conversion Noise Analysis

The actual mathematics used to calculate the noise result (Ansoft Serenade 8.*x*) is as follows [19],

k^{th} harmonic PM noise:

$$\left\langle \left|\delta\Phi_k(\omega)\right|^2 \right\rangle = \frac{N_k(\omega) - N_{-k}(\omega) - 2\,\mathrm{Re}\left[C_k(\omega)\right]}{R\left|I_k^{SS}\right|^2} \tag{3}$$

k^{th} harmonic AM noise:

$$\left\langle \left|\delta A_k(\omega)\right|^2 \right\rangle = 2\,\frac{N_k(\omega) - N_{-k}(\omega) + 2\,\mathrm{Re}\left[C_k(\omega)\right]}{R\left|I_k^{SS}\right|^2} \tag{4}$$

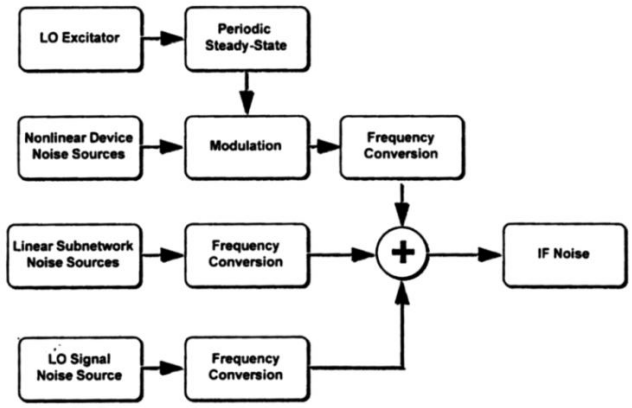

Figure 5 — Noise mechanisms.

k^{th} harmonic PM-AM correlation coefficient:

$$\begin{aligned} C_k^{PMAM}(\omega) &= \left\langle \delta\Phi_k(\omega)\delta A_k(\omega)^* \right\rangle \\ &= -\sqrt{2}\,\frac{2\,\mathrm{Im}\left[C_k(\omega)\right] + j\left[N_k(\omega) - N_{-k}(\omega)\right]}{R\left|I_k^{SS}\right|^2} \end{aligned} \tag{5}$$

where

$N_k(\omega)$, $N_{-k}(\omega)$ = noise power spectral densities at the upper and lower sidebands of the k^{th} harmonic

$C_k(\omega)$ = normalized correlation coefficient of the upper and lower sidebands of the k^{th} carrier harmonic

R = load resistance

I_k^{ss} = k^{th} harmonic of the steady-state current through the load.

Modulation Noise Analysis

k^{th} harmonic PM noise:

$$\left\langle \left|\delta\Phi_k(\omega)\right|^2 \right\rangle = \frac{k^2}{\omega^2}\mathbf{T}_F \left\rangle \mathbf{J}_H(\omega)\mathbf{J}_H^t(\omega) \right\langle \mathbf{T}_F^t \tag{6}$$

k^{th} harmonic AM noise:

$$\left\langle \left|\delta A_k(\omega)\right|^2 \right\rangle = \frac{2}{\left|I_k^{SS}\right|^2}\mathbf{T}_{Ak} \left\rangle \mathbf{J}_H(\omega)\mathbf{J}_H^t(\omega) \right\langle \mathbf{T}_{Ak}^t \tag{7}$$

k^{th} harmonic PM-AM correlation coefficient:

$$\begin{aligned} C_k^{PMAM}(\omega) &= \left\langle \delta\Phi_k(\omega)\delta A_k(\omega)^* \right\rangle \\ &= \frac{k\sqrt{2}}{j\omega\left|I_k^{SS}\right|^2}\mathbf{T}_F \left\rangle \mathbf{J}_H(\omega)\mathbf{J}_H^t(\omega) \right\langle \mathbf{T}_{Ak}^t \end{aligned} \tag{8}$$

where

$J_H(\omega)$ = vector of Norton equivalent of the noise sources

$\mathbf{T}_F$ = frequency transfer matrix

R = load resistance

I_k^{ss} = k^{th} harmonic of the steady-state current through the load.

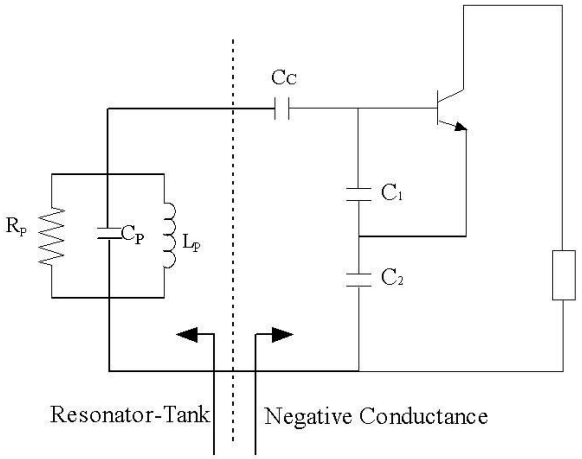

Figure 6 — Colpitts Oscillator configuration for the intrinsic case, no parasitics assumed, and an ideal transistor considered.

The following two circuits show the transition from a series tuned circuit connected with the series time-dependent negative resistance and the resulting input capacitance marked C_{IN}. Translated, the resulting configuration consists of a series circuit with inductance L and the resulting capacitance C'. The noise voltage $e_N(t)$ describes a small perturbation, which is the noise resulting from R_L and $-R_N(t)$. Figure 7 shows the equivalent representation of the oscillator circuit in the presence of noise.

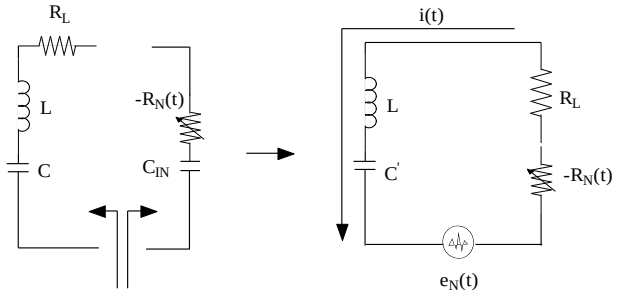

Figure 7 — Equivalent representation of the oscillator circuit in presence of noise.

The circuit equation of the oscillator circuit of Figure 7 can be given as

$$L\frac{di(t)}{dt}+(R_L-R_N(t))i(t)+\frac{1}{C'}\int i(t)dt=e_N(t) \qquad (9)$$

where $i(t)$ is the time varying resultant current. Due to the noise voltage $e_N(t)$, Equation (9) is a nonhomogeneous differential equation. If the noise voltage is zero, it translates into a homogeneous differential equation.

For a noiseless oscillator, the noise signal $e_N(t)$ is zero and the expression of the free-running oscillator current $i(t)$ can be assumed to be a periodic function of time and can be given as

$$i(t)=I_1\cos(\omega t+\varphi_1)+I_2\cos(2\omega t+\varphi_2) + I_3\cos(3\omega t+\varphi_3)+.....I_n\cos(n\omega t+\varphi_n) \qquad (10)$$

where I_1, I_2 …..I_n, are peak harmonic amplitudes of the current and φ_1, φ_2…..φ_n are time invariant phases.

In the presence of the noise perturbation $e_N(t)$, the current $i(t)$ may no longer be a periodic function of time and can be expressed as

$$i(t)=I_1(t)\cos[\omega t+\varphi_1(t)]+I_2(t)\cos[2\omega t+\varphi_2(t)]+ I_3(t)\cos[3\omega t+\varphi_3(t)]+ \ldots.I_{n-2}(t)\cos[(n-2)\omega t+\varphi_{n-2}(t)]+ I_{n-1}(t)\cos[(n-1)\omega t+\varphi_{n-1}(t)]+I_n(t)\cos[n\omega t+\varphi_n(t)] \qquad (11)$$

where $I_1(t)$, $I_2(t)$…..$I_n(t)$ are time variant amplitudes of the current and $\varphi_1(t)$, $\varphi_2(t)$…..$\varphi_n(t)$ are time variant phases.

Considering that $I_n(t)$ and $\varphi_n(t)$ do not change much over the period of $2\pi/n\omega$, each corresponding harmonic over one period of oscillation cycle remains small and more or less invariant. The solution of the differential equation becomes easy since the harmonics are suppressed due to a Q > 10, which prevents $i(t)$ to flow for the higher terms.

After the substitution of the value of di/dt and $\int i(t)dt$, the complete oscillator circuit equation, as given in Equation (9), can be rewritten as

$$\begin{aligned}&L\{\\&-I_1(t)(\omega+\frac{d\varphi_1(t)}{dt})\sin[\omega t+\varphi_1(t)]+\frac{dI_1(t)}{dt}\cos[\omega t+\varphi_1(t)]+\\&-I_2(t)(2\omega+\frac{d\varphi_2(t)}{dt})\sin[2\omega t+\varphi_2(t)]+\frac{dI_2(t)}{dt}\cos[2\omega t+\varphi_2(t)]+\\&-I_3(t)(3\omega+\frac{d\varphi_3(t)}{dt})\sin[3\omega t+\varphi_3(t)]+\frac{dI_3(t)}{dt}\cos[3\omega t+\varphi_3(t)]+\ldots\\&-I_n(t)(n\omega+\frac{d\varphi_n(t)}{dt})\sin[n\omega t+\varphi_n(t)]+\frac{dI_n(t)}{dt}\cos[n\omega t+\varphi_n(t)]\}+\\&[(R_L-R_N(t))i(t)]+\end{aligned}$$

$$\frac{1}{C'}\left\{\begin{array}{l}\left[\left[\frac{I_1(t)}{\omega}-\frac{I_1(t)}{\omega^2}\left(\frac{d\varphi_1(t)}{dt}\right)\right]\sin[\omega t+\varphi_1(t)]+\\ \frac{1}{\omega^2}\left(\frac{dI_1(t)}{dt}\right)\cos[\omega t+\varphi_1(t)]\end{array}\right\}+$$

$$\frac{1}{C'}\left\{\begin{array}{l}\left[\left[\frac{I_2(t)}{2\omega}-\frac{I_2(t)}{4\omega^2}\left(\frac{d\varphi_2(t)}{dt}\right)\right]\sin(2\omega t+\varphi_2(t)\right.\\ +\frac{1}{4\omega^2}\left(\frac{dI_2(t)}{dt}\right)\cos(2\omega t+\varphi_2(t))\end{array}\right\}+$$

$$\frac{1}{C'}\left\{\begin{array}{l}\left[\left[\frac{I_3(t)}{3\omega}-\frac{I_3(t)}{9\omega^2}\left(\frac{d\varphi_3(t)}{dt}\right)\right]\sin[3\omega t+\varphi_3(t)]+\\ \frac{1}{9\omega^2}\left(\frac{dI_3(t)}{dt}\right)\cos[3\omega t+\varphi_3(t)]\end{array}\right\}+\ldots$$

$$\frac{1}{C'}\left\{\begin{array}{l}\left[\left[\frac{I_n(t)}{n\omega}-\frac{I_n(t)}{n^2\omega^2}\left(\frac{d\varphi_n(t)}{dt}\right)\right]\sin[n\omega t+\varphi_n(t)]\right.\\ +\frac{1}{n^2\omega^2}\left(\frac{dI_n(t)}{dt}\right)\cos[n\omega t+\varphi_n(t)]\end{array}\right\}=e_N(t) \quad (12)$$

Because Q > 10 we approximate:

$$\frac{di(t)}{dt}=-I_1(t)(\omega+\frac{d\varphi_1(t)}{dt})\sin[\omega t+\varphi_1(t)]$$
$$+\frac{dI_1(t)}{dt}\cos[\omega t+\varphi_1(t)]+$$

+ (a slowly varying function at higher order harmonics of a very small amount).

$$\int i(t)dt=\left[\frac{I_1(t)}{\omega}-\frac{I_1(t)}{\omega^2}\left(\frac{d\varphi_1(t)}{dt}\right)\right]\sin[\omega t+\varphi_1(t)]$$

$$+\frac{1}{\omega^2}\left(\frac{dI_1(t)}{dt}\right)\cos[\omega t+\varphi_1(t)]+$$

+ (a slowly varying function at higher order harmonics of a very small amount).

After the substitution of the value of di/dt and $\int i(t)dt$, the oscillator circuit Equation (12) can be rewritten as

$$L\left[\begin{array}{l}-I_1(t)(\omega+\frac{d\varphi_1(t)}{dt})\sin[\omega t+\varphi_1(t)]\\ +\frac{dI_1(t)}{dt}\cos[\omega t+\varphi_1(t)]\end{array}\right]+\left[(R_L-R_N(t))I(t)\right]+$$

$$\frac{1}{C}\left\{\begin{array}{l}\left[\left[\frac{I_1(t)}{\omega}-\frac{I_1(t)}{\omega^2}\left(\frac{d\varphi_1(t)}{dt}\right)\right]\sin[\omega t+\varphi_1(t)]\right]\\ +\frac{1}{\omega^2}\left(\frac{dI_1(t)}{dt}\right)\cos[\omega t+\varphi_1(t)]\end{array}\right\}=e_N(t) \quad (13)$$

Following [18], and for simplification purposes, the equations above are multiplied with $\sin[\omega t+\varphi_1(t)]$ or $\cos[\omega t+\varphi_1(t)]$ and integrated over one period of the oscillation cycle, which will give an approximate differential equation for phase $\varphi(t)$ and amplitude $i(t)$ as

$$\left[\frac{2}{IT_0}\right]\int_{t-T_0}^{t}e_N(t)\sin[\omega t+\varphi(t)]dt$$
$$=-\frac{d\varphi}{dt}\left[L+\frac{1}{\omega^2C'}\right]+\left[-\omega L+\frac{1}{\omega C'}\right] \quad (14)$$

$$\left[\frac{2}{T_0}\right]\int_{t-T_0}^{t}e_N(t)\cos[\omega t+\varphi(t)]dt$$
$$=\frac{dI(t)}{dt}\left[L+\frac{1}{\omega^2C'}\right]+\left[R_L-\overline{R_N(t)}\right]I(t) \quad (15)$$

where $\overline{R_N(t)}$ is the average negative resistance under large signal condition.

$$\overline{R_N(t)}=\left[\frac{2}{T_0I}\right]\int_{t-T_0}^{t}R_N(t)I(t)\cos^2[\omega t+\varphi)]dt \quad (16)$$

Since the magnitude of the higher harmonics are not significant, the subscript of $\varphi(t)$and $I(t)$are dropped. Based on [18], we now determine the negative resistance.

Calculation of the Region of the Nonlinear Negative Resistance

Under steady-state free running oscillation condition,

$$\frac{dI(t)}{dt}\to 0$$

implies steady current, and

$$e_N(t)\to 0$$

with I is the fundamental RF current. Solving the now homogeneous differential equation for R_L - $R_N(t)$ and inserting the two terms into 15, we obtain

$$\left[\frac{2}{T_0}\right]\int_{t-T_0}^{t}e_N(t)\cos[\omega t+\varphi(t)]dt=$$
$$\frac{dI}{dt}\left[L+\frac{1}{\omega^2C'}\right]+\left[R_L-\overline{R_N(t)}\right]I(t) \quad (17)$$

term $\to 0$

now we introduce

γ; $\gamma = \Delta R/\Delta I$; for $\Delta\to 0$, $\gamma\to 0$

and $[R_L-\overline{R_N(t)}]=\gamma\ \Delta I$

$$\gamma\to 0\Rightarrow[R_L-\overline{R_N(t)}]I(t)\to 0 \quad (18)$$

$$R_L - \overline{R_N(t)} = R_{Load} - \left[\frac{2}{T_0}\right]\int_{t-T_0}^{t} R_N(t)\cos^2[\omega t + \varphi(t)]dt \to 0 \quad (19)$$

$[R_L - \overline{R_N(t)}]I(t) \to 0$ gives the intersection of $[\overline{R_N(t)}]$and $[R_L]$. This value is defined as I_0 which is the minimum value of the current needed for the steady-state sustained oscillation condition.

Figure 8 shows the plot of the nonlinear negative resistance, which is a function of the amplitude of the RF current. As the RF amplitude gets larger the conducting angle becomes narrower.

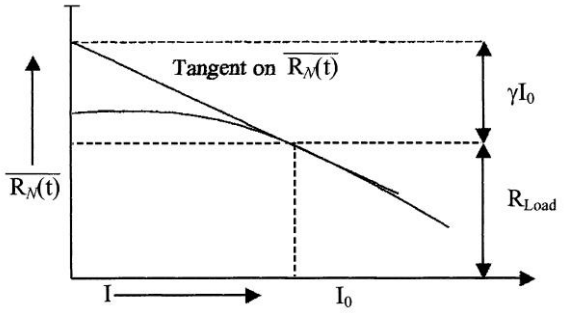

Figure 8 — Plot of negative resistance of $[\overline{R_N(t)}]$ *vs.* amplitude of current *I*.

For a small variation of the current ΔI from I_0, the relation above is expressed as

$$[R_L - \overline{R_N(t)}] = \gamma\ \Delta I \quad (20)$$

$\gamma\,\Delta I$ can be found from the intersection on the vertical axis by drawing the tangential line on $[\overline{R_N(t)}]$ at $I = I_0$. $|\Delta I|$ decreases exponentially with time for $\gamma > 0$.

Hence, I_0 represents the stable operating point. On the other hand, if $[\overline{R_N(t)}]$ intersects $[R_L]$ from the other side for $\gamma<0$ then $|\Delta I|$ grows indefinitely with time. Such an operating point does not support stable operation [18].

Calculation of the Noise Signal in Time Domain

From solving the two orthogonal equations, we need to obtain information about current $I(t)$ and $\varphi(t)$.

$$\left[\frac{2}{IT_0}\right]\int_{t-T_0}^{t} e_N(t)\sin[\omega t + \varphi(t)]dt = -\frac{d\varphi(t)}{dt}\left[L + \frac{1}{\omega^2 C'}\right] + \left[-\omega L + \frac{1}{\omega C'}\right] \quad (21)$$

$$\left[\frac{2}{T_0}\right]\int_{t-T_0}^{t} e_N(t)\cos[\omega t + \varphi(t)]dt = \frac{dI(t)}{dt}\left[L + \frac{1}{\omega^2 C'}\right] + \left[R_L - \overline{R_N(t)}\right]I(t) \quad (22)$$

The analysis of the noise signal can be accomplished by decomposing the noise signal $e_N(t)$ to an infinite number of random noise pulses represented by

$$\varepsilon\,\delta(t - t_0) \quad (23)$$

where ε is the strength of the pulse at the time instant t_0, and both ε and t_0 are independent random variables from one pulse to next pulse!

The time average of the square of the current pulses over a period of time can be shown to be

$$\frac{1}{2T}\int_{-T}^{T}\left[\sum \varepsilon\,\delta(t - t_0)\right]^2 dt = \overline{e_N^2(t)} \quad (24)$$

The mean square noise voltage $\overline{e_N^2(t)}$ is generated in the circuit in Figure 7.

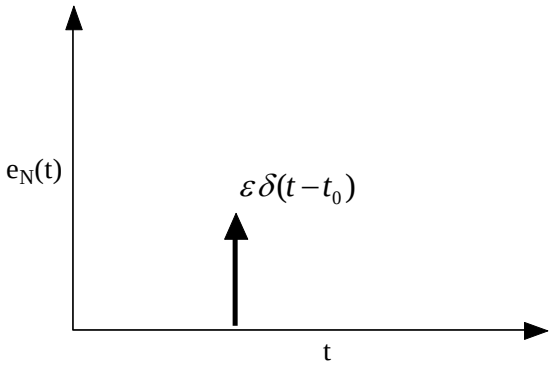

Figure 9 — The noise pulse at $I = t_0$.

Figure 9 shows the noise pulse at time instant $t = t_0$.

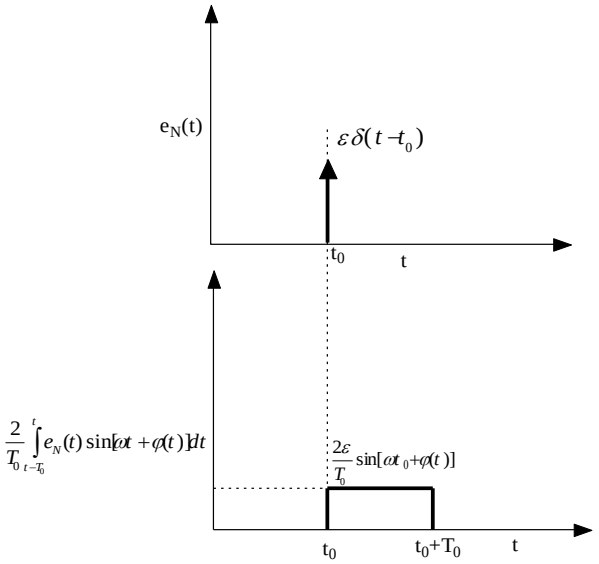

Figure 10 — The amplitude of the rectangular pulse.

The integral of the single noise pulse above gives the rectangular pulse with the height $\left[\frac{2}{T_0}\right]\varepsilon\sin[\omega t+\varphi(t)]$ and the length of T_0 as shown in Figure 10.

The integration of the single elementary noise pulse, following the Dirac Δ function, results in

$$\left[\frac{2}{T_0}\right]\int_{t-T_0}^{t} e_N(t)\sin[\omega t+\varphi(t)]dt \tag{25}$$

$$\approx\left[\frac{2}{T_0}\right]\int_{t-T_0}^{t}\varepsilon\,\delta(t-t_0)\sin[\omega t+\varphi(t)]dt]$$

$$\left[\frac{2}{T_0}\right]\int_{t-T_0}^{t}\varepsilon\,\delta(t-t_0)\sin[\omega t+\varphi(t)]dt \tag{26}$$

$$\approx\left[\frac{2}{T_0}\right]\varepsilon\sin[\omega t_0+\varphi(t)]$$

since the length of time T_0 is considered to be sufficiently small for any variation of $\varphi(t)$and $I(t)$ during the time T_0. The corresponding rectangular pulse of the magnitude $\frac{2}{T_0}\varepsilon\sin[\omega t_0+\varphi(t)]$ is considered to be another pulse located at $t = t_0$ and can be expressed in the form of an impulse function with the amplitude $2\varepsilon\sin[\omega t_0+\varphi(t)$ located at $t = t_0$ for calculating the effect using Equations (21) and (22).

The effect of $\left[\frac{2}{T_0}\right]\int_{t-T_0}^{t} e_N(t)\sin[\omega t+\varphi(t)]dt$ is given by $[n_1(t)]$ which consists of a number of rectangular pulses. The time average of the square of these pulses, following [18], can be calculated as

$$\frac{1}{2T}\int_{t=-T}^{t=T}\left[\sum 2\varepsilon\,\sin(\omega t_0+\varphi(t))\delta(t-t_0)\right]^2 dt \tag{27}$$

$$=\frac{1}{T}\int_{t=-T}^{t=T}\left[\sum\varepsilon\,\delta(t-t_0)\right]^2 dt$$

$$\overline{e_N^2(t)}=\frac{1}{2T}\int_{-T}^{T}\left[\sum\varepsilon\,\delta(t-t_0)\right]^2 dt \tag{28}$$

From the equation above,

$$\overline{n_1^2(t)}=2\overline{e_N^2(t)} \tag{29}$$

Similarly, the total response of $\frac{2}{T_0}\int_{t-T_0}^{t} e_N(t)\cos[\omega t+\varphi(t)]dt$ can be expressed by $[n_2(t)]$, which consists of a large number of such pulses and the time average of the square of these pulses is

$$\overline{n_2^2(t)}=2\overline{e_N^2(t)} \tag{30}$$

since $\frac{2}{T_0}\int_{t-T_0}^{t} e_N(t)\sin[\omega t+\varphi(t)]dt$

and $\frac{2}{T_0}\int_{t-T_0}^{t} e_N(t)\cos[\omega t+\varphi(t)]dt$ are orthogonal functions, and in the frequency domain are the upper and lower side bands relative to the carrier, and the correlation of $[n_1(t)]$ and $[n_2(t)]$ is

$$\overline{n_1(t)n_2(t)}=0 \tag{31}$$

Now consider the narrow band noise signal, which is

$$e_N(t)=e_{N1}(t)+e_{N2}(t) \tag{32}$$

$$e_{N1}(t)=e_1(t)\sin[\omega_0 t+\varphi(t)] \tag{33}$$

$$e_{N2}(t)=-e_2(t)\cos[\omega_0 t+\varphi(t)] \tag{34}$$

where $e_{N1}(t)$ and $e_{N2}(t)$ are orthogonal functions, and $e_1(t)$ and $e_2(t)$ are slowly varying functions of time.

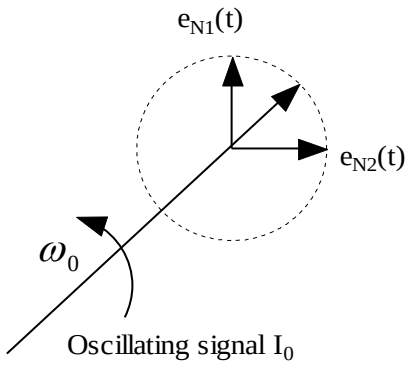

Figure 11 — Vector presentation of the oscillator signal and its modulation by the voltage e_{N1} and e_{N2}.

The calculation of $I_n(t)$ and $\varphi_n(t)$ for the free running oscillator can be derived from Equations (21) and (22) as

$$\left[\frac{2}{IT_0}\right]\int_{t-T_0}^{t} e_N(t)\sin[\omega t+\varphi(t)]dt \tag{35}$$

$$=-\frac{d\varphi(t)}{dt}\left[L+\frac{1}{\omega^2 C}\right]+\left[-\omega L+\frac{1}{\omega C}\right]$$

$$\left[\frac{2}{IT_0}\right]\int_{t-T_0}^{t} e_N(t)\sin[\omega t+\varphi(t)]dt \Rightarrow \left[\frac{1}{I}\right]n_1(t) \tag{36}$$

at resonance frequency $\omega = \omega_0$,

$$\left\{-\frac{d\varphi(t)}{dt}\left[L+\frac{1}{\omega^2 C}\right]+\left[-\omega L+\frac{1}{\omega C}\right]\right\}_{\omega=\omega_0} \tag{37}$$

$$= -2L\frac{d\varphi(t)}{dt}$$

and

$$\frac{1}{I}n_1(t) = -2L\frac{d\varphi(t)}{dt} \tag{38}$$

$$\frac{d\varphi(t)}{dt} = -\left[\frac{1}{2LI}\right]n_1(t) \tag{39}$$

If Equation (39) is transformed in the frequency domain, $\varphi(t)$ can be expressed as

$$\varphi(f) = \frac{n_1(f)}{2\omega LI} \tag{40}$$

Now the spectral density of $[\varphi(f)]$ is

$$|\varphi(f)|^2 = \frac{1}{4\omega^2 L^2 I^2}|n_1(f)|^2 \tag{41}$$

$$\frac{1}{4\omega^2 L^2 I^2}|n_1(f)|^2 = \frac{2|e_N(f)|^2}{4\omega^2 L^2 I^2} \tag{42}$$

$$\Rightarrow |\varphi(f)|^2 = \frac{2|e_N(f)|^2}{4\omega^2 L^2 I^2}$$

where f varies from $-\infty$ to $+\infty$.

The amplitude of the current can be written as $I(t) = I_0 + \Delta I(t)$, where I_0 represents the stable operating point of the free-running oscillator with a loop gain slightly greater than 1.

From Equation (22), we can calculate

$$\frac{2}{T_0}\int_{t-T_0}^{t} e_N(t)\cos[\omega t+\varphi(t)]dt$$

$$= \frac{dI(t)}{dt}\left(L+\frac{1}{\omega^2 C}\right)+\left[R_L-\overline{R_N(t)}\right]I(t),$$

$$\left[\frac{2}{T_0}\int_{t-T_0}^{t} e_N(t)\cos[\omega t+\varphi(t)]dt\right]_{\omega=\omega_0} \tag{43}$$

$$= \left[2L\frac{\partial}{\partial t}[\Delta I(t)]+\Delta I(t)I_0\gamma+\Delta I^2(t)\gamma\right]$$

Since the amplitude of $\Delta I^2(t)$ is negligible, its value can be set to 0;

$$\left[2L\frac{\partial}{\partial t}[\Delta I(t)]+\Delta I(t)I_0\gamma+\Delta I^2(t)\gamma\right] \tag{44}$$

$$= 2L\frac{\partial}{\partial t}[\Delta I(t)]+\Delta I(t)I_0\gamma$$

$$n_2(t) = \frac{2}{T_0}\int_{t-T_0}^{t} e_N(t)\cos[\omega t+\varphi(t)]dt \tag{45}$$

$$n_2(t) = 2L\frac{\partial}{\partial t}[\Delta I(t)]+\Delta I(t)I_0\gamma \tag{46}$$

$$n_2(f) = 2L\omega\,\Delta I(f)+\Delta I(f)I_0\gamma \tag{47}$$

The spectral density of [$n_2(f)$] is

$$|n_2(f)|^2 = [4L^2\omega^2+(I_0\gamma)^2]|\Delta I(f)|^2 \tag{48}$$

and the spectral density of $\Delta I(f)$ can be expressed in terms of $|n_2(f)|^2$ as

$$|\Delta I(f)|^2 = \frac{1}{[4L^2\omega^2+(I_0\gamma)^2]}|n_2(f)|^2 \tag{49}$$

$$|n_2(f)|^2 = 2|e_N(f)|^2$$
$$\Rightarrow |\Delta I(f)|^2 = \frac{2|e_N(f)|^2}{[4L^2\omega^2+(I_0\gamma)^2]} \tag{50}$$

since $n_1(t)$ and $n_2(t)$ are orthogonal function and there is no correlation between current and phase

$$\overline{n_1(t)n_2(t)} = 0 \Rightarrow \overline{I(t)\varphi(t)} = 0 \tag{51}$$

The output power noise spectral density of the current is given as

$$P_{noise}(f) = 2R_L|I(f)|^2 \tag{52}$$

The noise spectral density of the current is given as

$$|I(f)|^2 = \int_{-\infty}^{\infty} R_I(\tau)\exp(-j\omega\tau)d\tau \tag{53}$$

where $R_I(\tau)$ is the auto-correlation function of the current and can be written as

$$R_I(\tau)=\overline{\begin{bmatrix} I(t)I(t+\tau)\cos[\omega_0 t+\varphi(t)]\cos[\omega_0(t+\tau) \\ +\varphi(t+\tau)] \end{bmatrix}} \tag{54}$$

$$R_I(\tau)=\frac{1}{2}\left[I_0^2+R_{\Delta I}(\tau)\right]\cos(\omega_0\tau)[\overline{\cos(\varphi(t+\tau)-\varphi(t))}] \tag{55}$$

Since $I(t)$ and $\varphi(t)$ are uncorrelated, auto-correlation function o f the current $R_I(\tau)$ can be given as

From [18], but taking into consideration that both side bands are correlated, we can write

$$R_I(\tau)=\frac{1}{2}\left[I_0^2+\frac{2|e_N(\tau)|^2}{2L\gamma I_0}\exp\left(-\frac{\gamma I_0}{2L}|\tau|\right)\right] \tag{56}$$

$$\exp\left(-\frac{|e_N(\tau)|^2}{4L^2I_0^2}|\tau|\right)\cos(\omega_0\tau)$$

Since the publication [18] skipped many stages of the calculation, up to here, a more complete and detailed flow is shown. These results are needed to calculate the noise performance at the component level later. Note the factor of 2, which results from the correlation.

Considering $\frac{\gamma I_0}{2L} >> \frac{2|e_N(\tau)|^2}{4L^2I_0^2}$, the noise spectral density of the current is given by

$$|I(f)|^2=\int_{-\infty}^{\infty}R_I(\tau)\exp(-j\omega\tau)d\tau \tag{57}$$

with $I = I_0 + \Delta I(t)$; all RF-currents.

$$|I(f)|^2=\frac{|e_N(f)|^2}{8L^2}\left[\frac{1}{(\omega-\omega_0)^2+\left(\frac{|e_N(f)|^2}{4L^2I_0^2}\right)^2}+\frac{1}{(\omega+\omega_0)^2+\left(\frac{|e_N(f)|^2}{4L^2I_0^2}\right)^2}\right]+$$

$$\frac{|e_N(f)|^2}{8L^2}\left[\frac{1}{(\omega-\omega_0)^2+\left(\frac{\gamma I_0}{2L}\right)^2}+\frac{1}{(\omega+\omega_0)^2+\left(\frac{\gamma I_0}{2L}\right)^2}\right] \tag{58}$$

With

$$\frac{|e_N(f)|^2}{8L^2}\left[\frac{1}{(\omega-\omega_0)^2+\left(\frac{|e_N(f)|^2}{4L^2I_0^2}\right)^2}+\frac{1}{(\omega+\omega_0)^2+\left(\frac{|e_N(f)|^2}{4L^2I_0^2}\right)^2}\right]\rightarrow \text{FM noise} \tag{59}$$

$$\frac{|e_N(f)|^2}{8L^2}\left[\frac{1}{(\omega-\omega_0)^2+\left(\frac{\gamma I_0}{2L}\right)^2}+\frac{1}{(\omega+\omega_0)^2+\left(\frac{\gamma I_0}{2L}\right)^2}\right]\rightarrow \text{AM noise} \tag{60}$$

Since

$$\frac{\gamma I_0}{2L} >> \frac{2|e_N(\tau)|^2}{4L^2I_0^2}$$

for $\omega\rightarrow\omega_0$, FM noise predominates over the AM noise.

For $\omega>>\omega_0$, both the FM noise and AM noise terms give equal contribution.

Considering $\omega+\omega_0>>\omega-\omega_0$, then

$$|I(f)|^2=\frac{|e_N(f)|^2}{8L^2}\left[\frac{1}{(\omega-\omega_0)^2+\left(\frac{|e_N(f)|^2}{4L^2I_0^2}\right)^2}+\frac{1}{(\omega-\omega_0)^2+\left(\frac{\gamma I_0}{2L}\right)^2}\right] \tag{61}$$

$$P_{noise}(f)=2R_L|I(f)|^2 \tag{62}$$

$$P_{noise}(f)=2R_L\left(\frac{|e_N(f)|^2}{8L^2}\right)\left[\frac{1}{(\omega-\omega_0)^2+\left(\frac{|e_N(f)|^2}{4L^2I_0^2}\right)^2}+\frac{1}{(\omega-\omega_0)^2+\left(\frac{\gamma I_0}{2L}\right)^2}\right] \tag{63}$$

Since $R_{Load}=R_L+R_o$, the effective dynamic resistance of the free running oscillator is given by

$$\sum_{effective}|R_{tot}|=R_N(t)-R_{Load}]=R_o \tag{64}$$

where R_o is the output resistance; $R_0 - R_{tot} = 0$.

The Q of the resonator circuit is expressed as

$$Q_L = \frac{\omega L}{R_0} \tag{65}$$

The oscillator output noise power in terms of Q is given by

$$P_{noise}(f) = \frac{\omega_0^2}{2Q_L^2}\frac{|e|^2}{2\overline{R_N(t)}}\left[\frac{1}{(\omega-\omega_0)^2+\left(\frac{\omega_0^2}{4Q_L^2}\right)^2\left(\frac{|e|^2}{2\overline{R_N(t)}P_{out}^2}\right)^2} + \frac{1}{(\omega-\omega_0)^2+\left(\frac{\omega_0^2}{Q_L^2}\right)\left(\frac{\gamma\ I_0}{2\overline{R_N(t)}}\right)^2}\right] \tag{66}$$

Figure 12 shows the Colpitts oscillator with a series resonator and the small signal ac equivalent circuit.

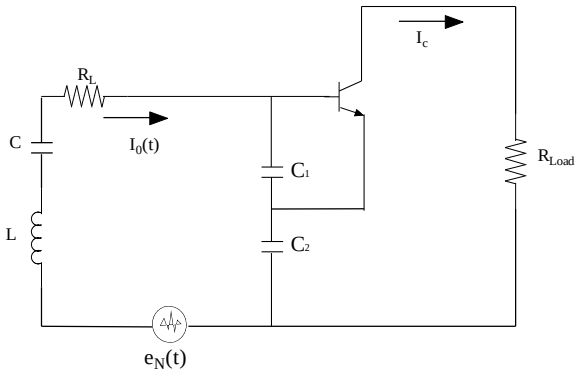

Figure 12 — Colpitts oscillator with series resonator and small signal ac equivalent circuit.

From the analytical expression of the noise analysis above, the influence of the circuit components on the phase noise can be explicitly calculated as

$$|\varphi(f)|^2 = \frac{1}{4\omega^2 L^2 I_0^2(f)}|n_1(f)|^2 \tag{67}$$

$$\frac{1}{4\omega^2 L^2 I_0^2(f)}|n_1(f)|^2 = \frac{2|e_N(f)|^2}{4\omega^2 L^2 I_0^2(f)}$$
$$\Rightarrow |\varphi(f)|^2 = \frac{2|e_N(f)|^2}{4\omega^2 L^2 I_0^2(f)} \tag{68}$$

where the frequency f varies from $-\infty$ to $+\infty$.

The resulting single sideband phase noise is

$$\pounds = \frac{|e_N(f)|^2}{4\omega^2 L^2 I_0^2(f)} \tag{69}$$

The unknown variables are $|e_N(f)|^2$ and $I_0^2(f)$, which need to be determined next. $I_0^2(f)$ will be transformed into $I_{c0}^2(f)$ by multiplying $I_0^2(f)$ with the effective current gain $Y_{21}^+/Y_{11}^+ = \beta^+$.

Calculation of $I_{c0}^2(f)$

From Figure 12, the LC-series resonant circuit is in shunt between the base and the emitter with the capacitive negative conductance portion of the transistor. We now introduce a collector load R_{Load} at the output, or better yet, an impedance Z.

The oscillator base current $i(t)$ is

$$i(t) = |I_0|\cos(\omega t) = \frac{V_{bc}(t)}{Z} \tag{70}$$

and the collector current is

$$|I_{c0}| = \left|\frac{[0.7 - V_{ce}]}{R_{Load} + j\left(\omega L - \frac{1}{\omega C_{IN}}\right)}\right| \tag{71}$$
$$\approx \left|\frac{V_{ce}}{R_{Load} + j\left(\omega L - \frac{1}{\omega C_{IN}}\right)}\right|$$

$$\overline{I_{c0}^2(f)} \approx \left\{\frac{\overline{V_{ce}^2(f)}}{[R_{Load}]^2 + \left(\omega L - \frac{1}{\omega C_{IN}}\right)^2}\right\} \tag{72}$$
$$= \left\{\frac{\overline{V_{ce}^2(f)}}{\left[\frac{\omega L}{Q}\right]^2 + \left(\omega L - \frac{1}{\omega C_{IN}}\right)^2}\right\}$$

The voltage V_{ce} is the RF voltage across the collector-emitter terminals of the transistor. Considering the steady-state oscillation $\omega \to \omega_0$, the total loss resistance is compensated by the negative resistance of the active device as $R_L = \overline{R_N(t)}$. The expression of $\left|\overline{I_{c0}^2(f)}\right|_{\omega=\omega_0}$ is

$$\left|\overline{I_{c0}^2(f)}\right|_{\omega=\omega_0} = \left|\frac{\overline{V_{ce}^2(f)}}{\left[\frac{\omega_0 L}{Q}\right]^2 + \left(\omega_0 L - \frac{1}{\omega_0 C_{IN}}\right)^2}\right| \tag{73}$$

$$= \left|\frac{\overline{V_{ce}^2(f)}}{(\omega_0 L)^2\left[\frac{1}{Q^2} + \left(1 - \frac{1}{\omega_0^2 LC_{IN}}\right)^2\right]}\right|$$

$$\left|\overline{I_{c0}^2(f)}\right|_{\omega=\omega_0}=\left|\frac{\overline{V_{ce}^2(f)}}{(\omega_0 L)^2\left[\frac{1}{Q^2}+\left(1-\frac{1}{\omega_0^2 L}\frac{C_1+C_2}{C_1C_2}\right)^2\right]}\right| \tag{74}$$

where C_{IN} is the equivalent capacitance of the negative resistor portion of the oscillator circuit.

$$C^{'}=\frac{CC_{IN}}{C+C_{IN}}, \qquad C_{IN}=\frac{C_1C_2}{C_1+C_2} \tag{75}$$

$$Q=\frac{\omega L}{R_L} \tag{76}$$

For a reasonably high Q resonator $\left|\overline{I_{c0}^2(f)}\right|_{\omega=\omega_0}\propto\left[C_{IN}\right]_{\omega=\omega_0}$

Calculation of the noise voltage $e_N(f)$

The equivalent noise voltage from the negative resistance portion of the oscillator circuit is given an open-circuit noise voltage [EMF] of the circuit as shown in Figure 13 below.

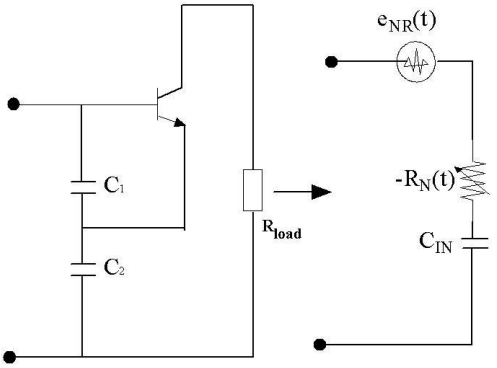

Figure 13 — Equivalent representation of negative resistance portion of the circuit at the input for the open circuit noise voltage.

The noise voltage associated with the resonator loss resistance R_s is

$$\left|\overline{e_R^2(f)}\right|_{\omega=\omega_0}=4kTBR_s \tag{77}$$

R_s denotes the equivalent series loss resistor, which can be calculated from the parallel loading resistor R_{load}, see Figure 12.

$$\left|\overline{e_R^2(f)}\right|_{\omega=\omega_0}=4kTR \text{ for } B = 1 \text{ Hz bandwidth} \tag{78}$$

The total noise voltage power within 1 Hz bandwidth can be given as

$$\left|\overline{e_N^2(f)}\right|_{\omega=\omega_0}=\overline{e_R^2(f)}+\overline{e_{NR}^2(f)} \tag{79}$$

Derivation of Equation (80):

The total noise voltage power within 1 Hz bandwidth can be given as

$$\left|\overline{e_N^2(f)}\right|_{\omega=\omega_0}=\overline{e_R^2(f)}+\overline{e_{NR}^2(f)} \tag{80}$$

The first term in Equation (80) is the noise voltage power due to the loss resistance R, and the second term is associated with the negative resistance of the active device R_N.

Figure 14 and 15 illustrate the oscillator circuit for the purpose of the calculation of the negative resistance.

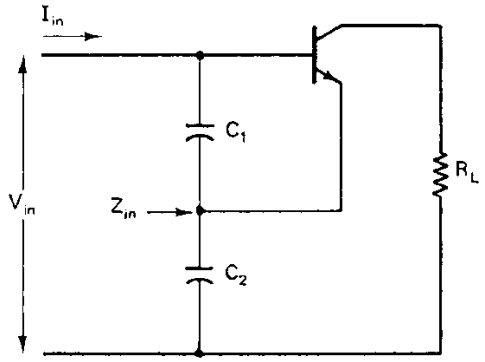

Figure 14 — Oscillator circuit for the calculation of the negative resistance.

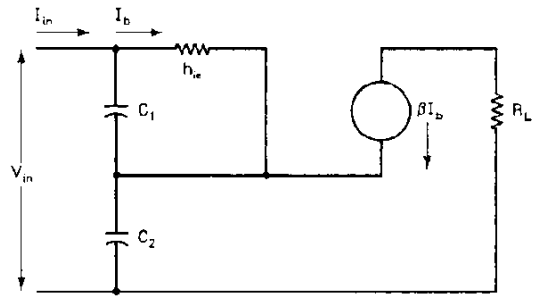

Figure 15 — Equivalent oscillator circuit for the calculation of the negative resistance.

From Figure 15, the circuit equation is given from Kirchoff's voltage law (KVL) as

$$V_{\text{in}}=I_{\text{in}}\left(X_{C_1}+X_{C_2}\right)-I_b\left(X_{C_1}-\beta X_{C_2}\right) \tag{81}$$

$$0=-I_{\text{in}}\left(X_{C_1}\right)+I_b\left(X_{C_1}+h_{ie}\right) \tag{82}$$

Considering, $\frac{1}{Y_{11}}=h_{ie}$

$$Z_{\text{in}}=\frac{V_{\text{in}}}{I_{\text{in}}}=\frac{(1+\beta)X_{C_1}X_{C_2}+h_{ie}\left(X_{C_1}+X_{C_2}\right)}{X_{C_1}+h_{ie}} \tag{83}$$

$$Z_{\text{in}} = \frac{\left(-\frac{(1+\beta)}{\omega^2 C_1 C_2} + \frac{(C_1+C_2)}{j\omega C_1 C_2}\frac{1}{Y_{11}}\right)}{\left(\frac{1}{Y_{11}} + \frac{1}{j\omega C_1}\right)} \tag{84}$$

$$Z_{\text{in}} = \frac{-jY_{11}(1+\beta) + \omega(C_1+C_2)}{\omega C_2(Y_{11} + j\omega C_1)} \tag{85}$$

$$Z_{\text{in}} = \frac{[\omega(C_1+C_2) - jY_{11}(1+\beta)][Y_{11} - j\omega C_1]}{\omega C_2(Y_{11}^2 + \omega^2 C_1^2)} \tag{86}$$

$$Z_{\text{in}} = \left[\frac{\omega Y_{11}(C_1+C_2) - (1+\beta)\omega C_1 Y_{11}}{\omega C_2(Y_{11}^2 + \omega^2 C_1^2)}\right] - j\left[\frac{Y_{11}^2(1+\beta) + \omega^2 C_1(C_1+C_2)}{\omega C_2(Y_{11}^2 + \omega^2 C_1^2)}\right] \tag{87}$$

$$Z_{\text{in}} = -R_n - jX \tag{88}$$

$$R_n = \frac{(1+\beta)\omega C_1 Y_{11} - \omega Y_{11}(C_1+C_2)}{\omega C_2(Y_{11}^2 + \omega^2 C_1^2)} = \frac{(1+\beta)C_1 Y_{11} - Y_{11}(C_1+C_2)}{C_2(Y_{11}^2 + \omega^2 C_1^2)} \tag{89}$$

$$R_n = \frac{\beta C_1 Y_{11} - Y_{11} C_2}{C_2(Y_{11}^2 + \omega^2 C_1^2)} = \frac{\beta Y_{11}}{\frac{C_2}{C_1}(Y_{11}^2 + \omega^2 C_1^2)} - \frac{Y_{11}}{(Y_{11}^2 + \omega^2 C_1^2)} \tag{90}$$

Considering $\beta = \frac{Y_{21}}{Y_{11}} \approx \frac{g_m}{Y_{11}}$

$$R_n = \frac{g_m}{\frac{C_2}{C_1}(\frac{g_m^2}{\beta^2} + \omega^2 C_1^2)} - \frac{g_m/\beta}{(\frac{g_m^2}{\beta^2} + \omega^2 C_1^2)} \tag{91}$$

$$R_n = \frac{g_m \beta^2 C_1}{(g_m^2 C_2 + \omega^2 \beta^2 C_1^2 C_2)} - \frac{g_m \beta}{(g_m^2 + \beta^2 \omega^2 C_1^2)} \tag{92}$$

$$R_n = \frac{g_m \beta^2 \omega^2 C_1 C_2}{\omega^2 C_1^2(\frac{C_2^2}{C_1^2} g_m^2 + \omega^2 \beta^2 C_2^2)} - \frac{g_m \beta \omega^2 C_2^2}{\omega^2 C_1^2(\frac{C_2^2}{C_1^2} g_m^2 + \beta^2 \omega^2 C_2^2)} \tag{93}$$

$$R_n = \left[\frac{g_m^2}{\omega^2 C_1^2(\frac{C_2^2}{C_1^2} g_m^2 + \omega^2 \beta^2 C_2^2)}\right]\left[\frac{\beta^2 \omega^2 C_1 C_2}{g_m} - \frac{\beta \omega^2 C_2^2}{g_m}\right] \tag{94}$$

$$R_n = \left[\frac{g_m^2}{\omega^2 C_1^2(\frac{C_2^2}{C_1^2} g_m^2 + \omega^2 \beta^2 C_2^2)}\right]\left[g_m\left[\left(\frac{\omega C_1}{Y_{11}}\right)\left(\frac{\omega C_2}{Y_{11}}\right) - \frac{\omega^2 C_2^2}{\beta Y_{11}^2}\right]\right] \tag{95}$$

$$R_n = \left[\frac{g_m^2}{\omega^2 C_1^2(\frac{C_2^2}{C_1^2} g_m^2 + \omega^2 \beta^2 C_2^2)}\right]\left[g_m\left[\left(\frac{\omega C_1}{Y_{11}}\right)\left(\frac{\omega C_2}{Y_{11}}\right) - \frac{1}{\beta}\left(\frac{\omega C_2}{Y_{11}}\right)\left(\frac{\omega C_2}{Y_{11}}\right)\right]\right] \tag{96}$$

Considering $\left(\frac{\omega C_1}{Y_{11}}\right)\left(\frac{\omega C_2}{Y_{11}}\right) >> \frac{1}{\beta}\left(\frac{\omega C_2}{Y_{11}}\right)\left(\frac{\omega C_2}{Y_{11}}\right)$

and $\left(\frac{\omega C_1}{Y_{11}}\right)\left(\frac{\omega C_2}{Y_{11}}\right) \approx 1$ (97)

$$\left[g_m\left[\left(\frac{\omega C_1}{Y_{11}}\right)\left(\frac{\omega C_2}{Y_{11}}\right) - \frac{1}{\beta}\left(\frac{\omega C_2}{Y_{11}}\right)\left(\frac{\omega C_2}{Y_{11}}\right)\right]\right] \tag{98}$$

$$\cong \frac{I_C}{V_T} = \frac{I_C}{kT/q} \Rightarrow \frac{qI_C}{kT}$$

From (96) and (98)

$$R_n = \left[\frac{g_m^2}{\omega^2 C_1^2(\frac{C_2^2}{C_1^2} g_m^2 + \omega^2 \beta^2 C_2^2)}\right]\frac{qI_C}{kT} \tag{99}$$

From (80), the total noise voltage power within a 1 Hz bandwidth can be given as

$$\left|\overline{e_N^2(f)}\right|_{\omega=\omega_0} = \overline{e_R^2(f)} + \overline{e_{NR}^2(f)} \tag{100}$$

$$\left|\overline{e_N^2(f)}\right|_{\omega=\omega_0} = [4kTR] + \left[\frac{4qI_c g_m^2 + \frac{K_f I_b^{AF}}{\Delta\omega} g_m^2}{\omega_0^2 C_1^2(\omega_0^2(\beta^+)^2 C_2^2 + g_m^2 \frac{C_2^2}{C_1^2})}\right] \tag{101}$$

where

$$\beta^+ = \left[\frac{Y_{21}^+}{Y_{11}^+}\right]\left[\frac{C_1}{C_2}\right]^p, \quad g_m = \left[Y_{21}^+\right]\left[\frac{C_1}{C_2}\right]^q, \text{ redefined} \tag{102}$$

where

The values of p and q depend upon the drive level.

The flicker noise contribution in Equation (80) is introduced by adding term $\frac{K_f I_b^{AF}}{\Delta\omega}$ in I_{c0}, where K_f is the flicker noise coefficient and AF is the flicker noise exponent. This is valid only for the bipolar transistor. For an FET, the equivalent currents have to be used.

In this case we use a value of 10^{-8}, some publications claim much smaller numbers such as 10^{-11}. The authors must have done some magic to get the measured curve fitted. In my opinion these small numbers violate the laws of physics for bipolar transistors.

The first term in the expression above is related to the thermal noise due to the loss resistance of the resonator tank and the second term is related to the shot noise and flicker noise in the transistor.

Now, the phase noise of the oscillator can be expressed as

$$\left|\overline{\varphi^2(\omega)}\right| = \frac{2\left|\overline{e_N^2(\omega)}\right|}{4\omega_0^2 L^2 I_0^2(\omega)} \tag{103}$$

$$\left|\overline{\varphi^2(\omega)}\right|_{SSB} = \frac{1}{2}\left|\overline{\varphi^2(\omega)}\right| = \frac{\left|\overline{e_N^2(\omega)}\right|}{4\omega_0^2 L^2 I_0^2(\omega)} \tag{104}$$

$$\left|\overline{\varphi^2(\omega)}\right|_{SSB} = \left\{\left[4kTR\right] + \left[\frac{4qI_c g_m^2 + \frac{K_f I_b^{AF}}{\omega} g_m^2}{\omega_0^2 C_1^2 (\omega_0^2 (\beta^+)^2 C_2^2 + g_m^2 \frac{C_2^2}{C_1^2})}\right]\right\} \tag{105}$$

$$\left[\frac{(\omega_0)^2\left[\frac{1}{Q^2} + \left(1 - \frac{1}{\omega_0^2 L}\frac{C_1 + C_2}{C_1 C_2}\right)^2\right]}{4\omega^2 \left|V_{ce}^2(\omega)\right|}\right]$$

$$\left|\overline{\varphi^2(\omega)}\right|_{SSB} = \left[4kTR + \left[\frac{4qI_c g_m^2 + \frac{K_f I_b^{AF}}{\omega} g_m^2}{\omega_0^2 C_1^2 (\omega_0^2 (\beta^+)^2 C_2^2 + g_m^2 \frac{C_2^2}{C_1^2})}\right]\right] \tag{104}$$

$$\left[\frac{\omega_0^2}{4\omega^2 V_{ce}^2}\right]\left[\frac{1}{Q^2} + \left(1 - \frac{1}{\omega_0^2 L}\frac{C_1 + C_2}{C_1 C_2}\right)^2\right]$$

Considering

$$\left(\frac{1}{\omega_0^2 L}\frac{C_1 + C_2}{C_1 C_2}\right) >> 1 \text{; for}$$

$\omega_0 = 2\pi f = 6.28\times10^{-9}$ Hz, $L = 10^{-9}$ H , $C_1 = 10^{-12}$ F, $C2 = 10^{-12}$ F

$$\left(\frac{1}{\omega_0^2 L}\frac{C_1 + C_2}{C_1 C_2}\right) = 50.7 \text{ .}$$

Since the phase noise is always expressed in dBc/Hz, we now calculate, after simplification of Equation (84),

$$\pounds(\omega) = 10\log\left\{\left[\left[4kTR + \left[\frac{4qI_c g_m^2 + \frac{K_f I_b^{AF}}{\omega} g_m^2}{\omega_0^2 C_1^2 (\omega_0^2 (\beta^+)^2 C_2^2 + g_m^2 \frac{C_2^2}{C_1^2})}\right]\right]\right.\right.$$
$$\left.\left.\left[\frac{\omega_0^2}{4\omega^2 V_{cc}^2}\right]\left[\frac{1}{Q^2} + \frac{[C_1 + C_2]^2}{C_1^2 C_2^2 \omega_0^4 L^2}\right]\right\}\right. \tag{107}$$

For the bias condition (which is determined from the output power requirement), the loaded quality factor, and the device parameters [transconductance and β^+], the best phase noise can be found by differentiating $\left|\overline{\varphi^2(\omega)}\right|_{SSB}$ with respect to C_1/C_2 .

Considering that all the parameters of $\left|\overline{\varphi^2(\omega)}\right|_{SSB}$ are constants for a given operating condition (except the feedback capacitor), the minimum value of the phase noise can be determined for any fixed value of C_1 as

$$\left|\overline{\varphi^2(\omega)}\right| = \left[k_0 + \frac{k_1}{k_2 C_1^2 C_2^2 + k_3 C_2^2}\right]\left[\frac{C_1 + C_2}{C_1 C_2}\right]^2 \tag{108}$$

$$k_0 = \frac{kTR}{\omega^2\, \omega_0^2 L^2 V_{ce}^2} \tag{109}$$

$$k_1 = \frac{qI_{c0} g_m^2 + \frac{K_f I_b^{AF}}{\omega} g_m^2}{\omega^2\, \omega_0^2 L^2 V_{ce}^2} \tag{110}$$

$$k_2 = \omega_0^4 (\beta^+)^2 \tag{111}$$

$$k_3 = g_m^2 \tag{112}$$

Where k_1, k_2, and k_3, are constant only for a particular drive level, with $y = C_1/C_2$. Making k_2 and k_3 also dependent on y, as the drive level changes, the final noise equation is

$$\pounds(\omega) = 10 \times \log\left[\left[k_0 + \left(\frac{k^3 k_1 \left[\frac{Y_{21}^+}{Y_{11}^+}\right]^2 [y]^{2p}}{\left[Y_{21}^+\right]^3 [y]^{3q}}\right)\right]\left[\frac{[1+y]^2}{y^2}\right]\right] \tag{113}$$
$$\left[\left(\frac{1}{(y^2 + k)}\right)\right]$$

where

$$k_0 = \frac{kTR}{\omega^2\,\omega_0^2 L^2 V_{cc}^2}$$

$$k_1 = \frac{qI_c g_m^2 + \dfrac{K_f I_b^{AF}}{\omega} g_m^2}{\omega^2\,\omega_0^4 L^2 V_{cc}^2}$$

$$k_2 = \omega_0^2 (\beta^+)^2$$

Figure 16 shows the simulated phase noise and its minimum for two values of C_1, 2 pF and 5 pF. 5 pF, provides a better phase noise and a flatter response. For larger C_1, the oscillator will cease to oscillate.

$$\frac{\partial \left|\phi^2(\omega, y, k)\right|}{\partial y} \Rightarrow 0$$

$$\frac{\partial}{\partial y}\left\{\left[k_0 + \left(\frac{k^3 k_1 \left[\dfrac{Y_{21}^+}{Y_{11}^+}\right]^2 [y]^{2p}}{\left[Y_{21}^+\right]^3 [y]^{3q}}\right)\left(\frac{1}{(y^2+k)}\right)\right]\left[\frac{[1+y]^2}{y^2}\right]\right\}_{y=m} \Rightarrow 0 \qquad (114)$$

From curve-fitting attempts, the following values for q and p in Equation (114) were determined:

q=1 to 1.1; p = 1.3 to 1.6.

q and p are a function of the normalized drive level x and need to be determined experimentally.

The transformation factor n is defined as

$$n = 1 + \frac{C_1}{C_2} \rightarrow 1 + y \qquad (115)$$

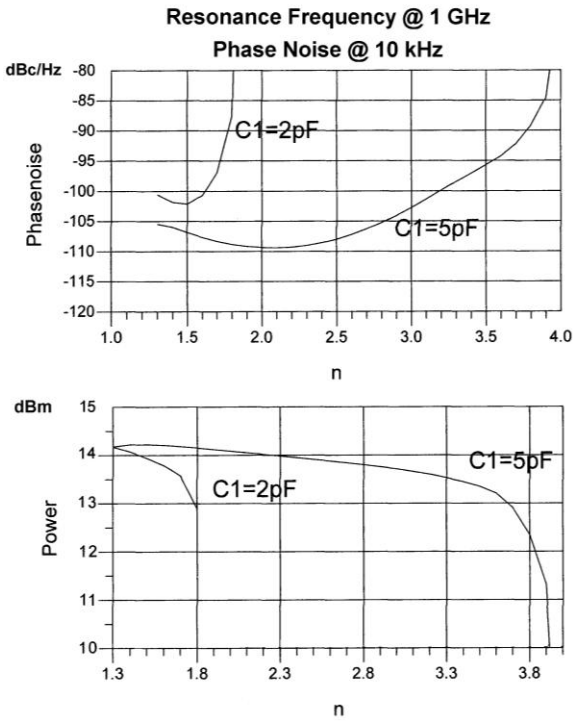

Figure 16 — Phase noise vs. *n* and output power.

The following plot in Figure 17 shows the predicted phase noise resulting from Equation (114). For the first time, the flicker corner frequency was properly implemented and gives answers consistent with the measurements. In the following chapter all the noise sources will be added, but the key contributors are still the resonator noise and the flicker noise. The Schottky noise dominates further out. The break point for the flicker noise can be clearly seen.

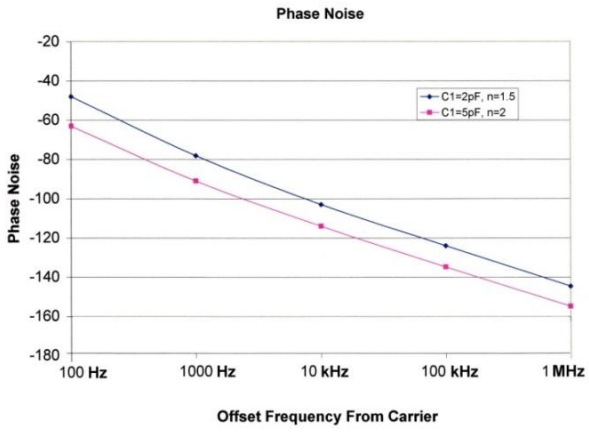

Figure 17 — Using Equation (114), the phase noise for different values of *n* for constant C_2 can be calculated.

Summary Results

The analysis of the oscillator in the time domain has given us a design criteria to find the optimum value of

$y = C_1/C_2$ with values for y + 1 (or n) ranging from 1.5 to 4. For values above 3.5, the power is reduced significantly.

Consistent with the previous chapters, we note

$$C_1 = C_1^* \pm X(C_P \text{ or } L_P) \tag{116}$$

$$X(C_{be} \text{ or } L_b) \rightarrow C_P \text{ or } L_P \tag{117}$$

In the case of a large value of C_P (C_P>C_1), X_1 has to be inductive to compensate extra contributions of the device package capacitance to meet the desired value of C_1!

The following is a set of design guides to calculate the parameters of the oscillator.

$$\omega = \sqrt{\frac{1}{L\left[\frac{C_1C_2}{C_1+C_2}+C\right]}} \tag{118}$$

$$\left|R_n(L_P=0)\right| = \frac{Y_{21}}{\omega^2 C_1 C_2} \tag{119}$$

$$C_1 = \frac{1}{\omega_0}\sqrt{\frac{Y_{11}}{K}} \tag{120}$$

C_2 is best be determined graphically from the noise plot.

$$C_C > \left\{\frac{(\omega^2 C_1C_2)(1+\omega^2 Y_{21}^2 L_P^2)}{[Y_{21}^2 C_2 - \omega^2 C_1 C_2)(1+\omega^2 Y_{21}^2 L_P^2)(C_1+C_P+C_2)]}\right\} \tag{121}$$

$$\frac{C}{10} \geq [C_C]_{L_P=0} > \left[\frac{(\omega^2 C_1C_2)}{[Y_{21}^2 C_2 - \omega^2 C_1 C_2)(C_1+C_P+C_2)]}\right] \tag{122}$$

The phase noise in dBc/Hz is shown as

$$\pounds(\omega) = 10 \times \log\left[\left[\left[k_0 + \left(\frac{k^3 k_1\left[\frac{Y_{21}^+}{Y_{11}^+}\right]^2 [y]^{2p}}{\left[Y_{21}^+\right]^3 [y]^{3q}}\right)\right]\left[\frac{[1+y]^2}{y^2}\right]\right]\left(\frac{1}{(y^2+k)}\right)\right] \tag{123}$$

The phase noise improves with the square of the loaded Q_L! 10% higher $Q \rightarrow$ 20% better phase noise!

$$L(\omega) \propto \frac{1}{C_{IN}^2} \tag{124}$$

The loaded Q of the resonator determines the minimum possible level of the oscillator phase noise for given bias voltage and oscillator frequency.

To achieve close to this minimum phase noise level set by the loaded Q_L of the resonator, the optimum (rather, how large the value of the C_{IN} can be) value of C_{IN} is to be fixed.

To achieve the best possible phase noise level, the feedback capacitors C_1 and C_2 should be made as large as possible, but still generate sufficient negative resistance for sustaining steady-state oscillation.

$$[-R_N]_{\substack{\text{negative}\\ \text{resistance}}} \propto \frac{1}{\omega_0^2}\frac{1}{C_1C_2}, \text{ (no parasitics)} \tag{125}$$

The negative resistance of the oscillator circuit is inversely proportional to the feedback capacitors. Therefore, the limit of the feedback capacitor value is determined by the minimum negative resistance for a loop gain greater than unity.

From the phase noise equation discussed, the feedback capacitor C_2 has more influence compared to C_1. The drive level and conduction angle of the Colpitts oscillator circuit is a strong function of C_2.

The time domain approach has provided us with the design guide for the key components of the oscillator; however, it did not include all the noise sources of the transistor. By using the starting parameters, such as C_1 and C_2 and the bias point, as well as the information about the resonator and the transistor, a complete noise model/analysis will now be shown.

The time domain approach has provided us with the design guide for the key components of the oscillator; however, it did not include all the noise sources of the transistor. By using the starting parameters, such as C_1 and C_2 and the bias point, as well as the information about the resonator and the transistor, a complete noise model/analysis will be shown now.

After some lengthy calculations and approximations, adding shot noise, flicker noise and the loss resistor, the equivalent expression of the phase noise can be derived as

$$\pounds(\omega) = \left[\begin{array}{c} \left|g_m^2(t)\right|(4qI_c) + \\ \left|g_m^2(t)\right|\left(\frac{K_f I_b^{AF}}{\omega}\right) \\ \hline \omega_0^4 \beta^2 C_{ce}^2 (C_2 + C_{b'e} - L_1C_2C_{be}\omega_0^2)^2 + \\ \left|g_m^2(t)\right|\omega_0^2 (C_2 + C_{b'e} - L_1C_2C_{b'e}\omega_0^2)^2 \end{array}\right] \times \tag{126}$$

$$\frac{\omega_0^2}{4\omega^2 V_{ce}^2}\left[\frac{Q_0^2}{Q_L^2} + \left(1 - \frac{1}{\omega_0^2 L_1}\left(\frac{[(C_2 + C_{b'e} - L_1C_2C_{b'e}\omega_0^2) + C_{ce}]}{C_{ce}[(C_2 + C_{b'e} - L_1C_2C_{b'e}\omega_0^2)]}\right)\right)^2\right]$$

The flicker noise contribution in equation (126) is introduced by adding term $K_f I_b^{AF} / \omega$ in RF collector current I_C, where K_f is the flicker noise coefficient and *AF* is the flicker noise exponent. This is valid only for the bipolar transistor. For an FET, the equivalent current transformations have to be used.

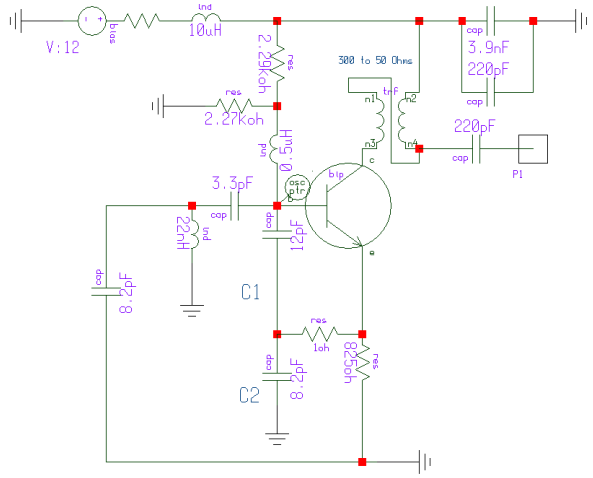

Figure 18 — Colpitts Configuration – Test Circuit.

This is the most complete noise model derived and tested.

Validation

After so many calculations a proof of concept is called for [14-20]. Figure 18 shows the test circuit. It is the typical Colpitts oscillator with the RF output taken from the collector. The transistor BFG 520 is made by Philips and is a 9 GHz NPN device used at a small fraction of I_C max.

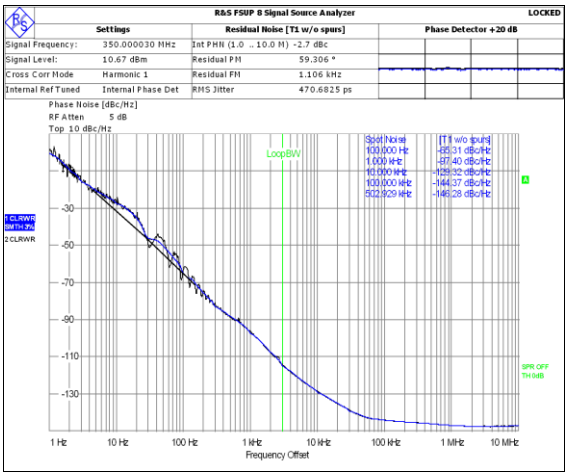

Figure 19: Measured Data for a 350MHz Oscillator.

The measured phase noise data is shown in Figure 19 and the simulated data in Figure 20. When applying the analytical noise equation we obtain good agreement with the actual measurements also.

This proves that the calculations are valid, any one need not spend $ 25,000 for a Harmonic Balance based simulator.

The phase noise, far out, is limited by the needed isolation/buffer stage.

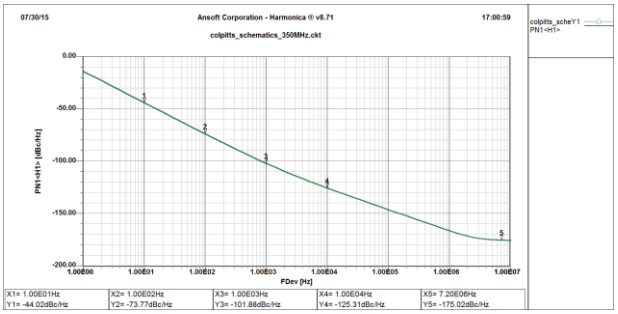

Figure 20 — Simulated Phase Noise Data for the test circuit of Figure 18.

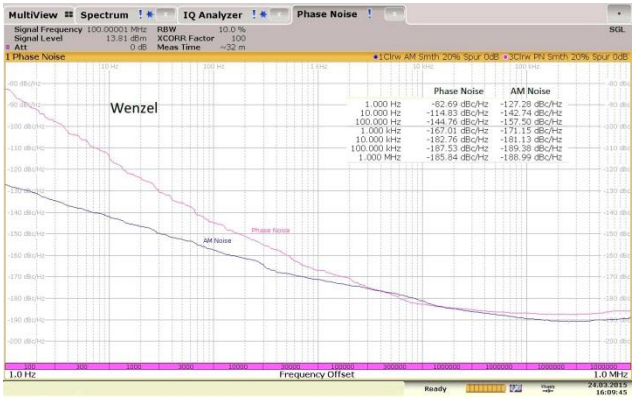

Figure 21 — Phase Noise Measurements (AM and FM noise) of a popular Wenzel 100 MHz Crystal Oscillator.

With the latest test equipment (R&S FSWP) FM and AM noise can be measured separately. Using a popular crystal oscillator at 100 MHz made by Wenzel, both AM and FM components can be inspected.

There is an area where the AM noise (unfortunately) is larger than the FM noise. That indicates the internal buffer stage is partially driven into saturation. By changing some component values this can be avoided.

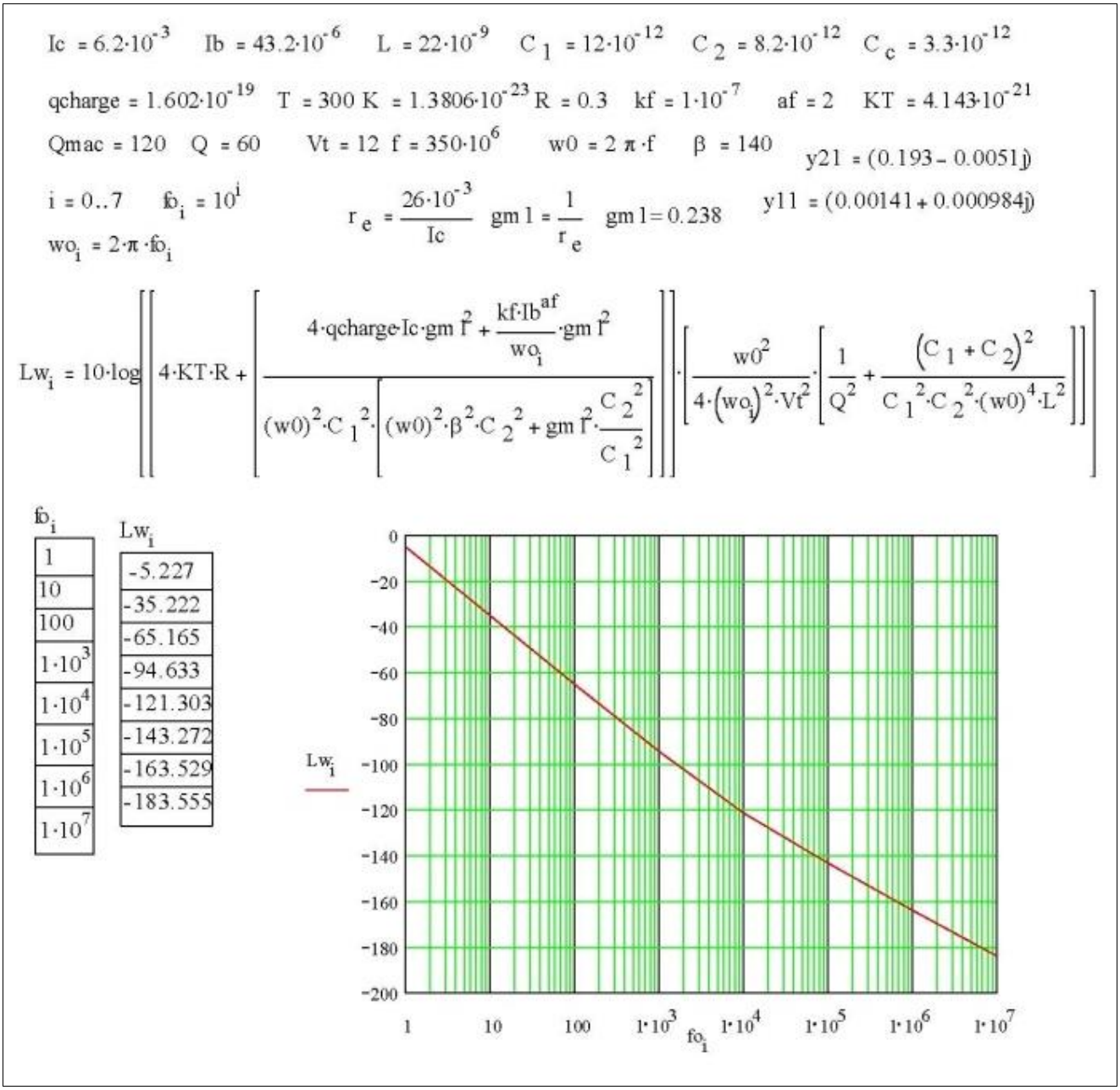

Figure 22 — Mathcad Worksheet for calculated Phase Noise of a 350 MHz Colpitts Oscillator.

The MathCad worksheet, **Eqn_107_350MHz.mcd** file, can be found at **www.arrl.org/QEXfiles**.

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Receiver Phase Noise Measurement

Phase Noise at Low Frequencies

No mixer has perfect port-to-port isolation, and some of a receiver's local-oscillator signal leaks through into the IF. If we tune a general-coverage receiver, with its antenna disconnected, to exactly 0 Hz, the local oscillator is exactly at the IF center frequency, and the receiver acts as if it is tuned to a very strong unmodulated carrier. A typical mixer might give only 40 dB of LO isolation and have an LO drive power of at least 10 mW. If we tune away from 0 Hz, the LO carrier tunes away from the IF center and out of the passband. The apparent signal level falls. Although this moves the LO carrier out of the IF passband, some of its noise sidebands will not be, and the receiver will respond to this energy as an incoming noise signal. To the receiver operator, this sounds like a rising noise floor as the receiver is tuned toward 0 Hz.

To get good noise floor at very low frequencies, some professional/military receivers, like the Racal RA1772, use very carefully balanced mixers to get as much port-to-port isolation as possible, and they also may switch a crystal notch filter into the first mixer's LO feed. Most general-coverage radios inhibit tuning in the LF or VLF region. It could be suggested by a cynic that how low manufacturers allow you to tune is an indication of how far they think their phase-noise sidebands could extend!

Phase Noise Measurements

There are several different ways of measuring phase noise, offering different tradeoffs between convenience, cost and effort. Some methods suit oscillators in isolation, others suit them in-situ (in their radios).

If you're unfamiliar with noise measurements, the units involved may seem strange. One reason for this is that a noise signal's power is spread over a frequency range, like an infinite number of infinitesimal sinusoidal components. This can be thought of as similar to painting a house. The area that a gallon of paint can cover depends on how thinly it's spread. If someone asks how much paint was used on some part of a wall, the answer would have to be in terms of paint volume per square foot. The wall can be considered to be an infinite number of points, each with an infinitesimal amount of paint applied to it. The question of what volume of paint has been applied at some specific point is unanswerable. With noise, we must work in terms of *power density*, of watts per hertz. We therefore express phase-noise level as a ratio of the carrier power to the noise's power density. Because of the large ratios involved, expression in decibels is convenient. It has been a convention to use *dBc* to mean "decibels with respect to the carrier."

For phase noise, we need to work in terms of a standard bandwidth, and 1 Hz is the obvious candidate. Even if the noise is measured in a different bandwidth, its equivalent power in 1 Hz can be easily calculated. A phase-noise level of –120 dBc in a 1-Hz bandwidth (often written as

"–120 dBc/Hz") translates into each hertz of the noise having a power of 10^{-12} of the carrier power. In a bandwidth of 3 kHz, this would be 3000 times larger.

The most convenient way to measure phase noise is to buy and use a commercial phase noise test system. Such a system usually contains a state-of-the-art, low-noise frequency synthesizer and a low-frequency spectrum analyzer, as well as some special hardware. Often, a second, DSP-based spectrum analyzer is included to speed up and extend measurements very close to the carrier by using the Fast Fourier Transform (FFT). The whole system is then controlled by a computer with proprietary software. With a good system like this costing about $100,000, this is not a practical method for amateurs, although a few fortunate individuals have access to them at work. These systems are also overkill for our needs, because we are not particularly interested in determining phase- noise levels very close to and very far from the carrier.

It's possible to make respectable receiver-oscillator phase-noise measurements with less than $100 of parts and a multimeter. Although it's time-consuming, the technique is much more in keeping with the amateur spirit than using a $100k system! An ordinary multimeter will produce acceptable results; a meter capable of indicating "true RMS" ac voltages is preferable because it can give correct readings on sine waves *and* noise. **Figure 1** shows the setup. Measurements can only be made around the frequency of the crystal oscillator, so if more than one band is to be tested, crystals must be changed, or else a set of appropriate oscillators is needed. The oscillator should produce about +10 dBm (10 mW) and be *very* well shielded. (To this end, it's advisable to build the oscillator into a die-cast box and power it from internal batteries. A noticeable shielding improvement results even from avoiding the use of an external power switch; a reed-relay element inside the box can be positioned to connect the battery when a small permanent magnet is placed against a marked place outside the box.)

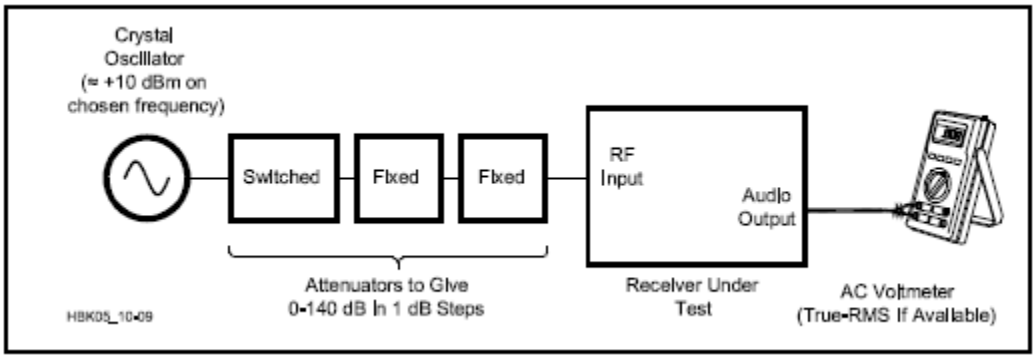


Figure 1 — Setup for measuring receiver-oscillator phase noise.

Likewise, great care must be taken with attenuator shielding. A total attenuation of around 140 dB is needed, and with so much attenuation in line, signal leakage can easily exceed the test signal that reaches the receiver. It's not necessary to be able to switch-select all 140 dB of the attenuation, nor is this desirable, as switches can leak. All of the attenuators' enclosure seams must be soldered. A pair of boxes with 30 dB of fixed attenuation each is needed to complete the

set. With 140 dB of attenuation, coax cable leakage is also a problem. The only countermeasure against this is to minimize all cable lengths and to interconnect test-system modules with BNC plug-to-plug adapters (UG-491A) where possible.

Ideally, the receiver could simply be tuned across the signal from the oscillator and the response measured using its signal-strength (S) meter. Unfortunately, receiver S meters are notoriously imprecise, so an equivalent method is needed that does not rely on the receiver's AGC system.

The trick is not to measure the response to a fixed level signal, but to measure the changes in applied signal power needed to give a fixed response. Here is a step-by-step procedure based on that described by John Grebenkemper, KI6WX, in March and April 1988 *QST*:

1. Connect the equipment as shown in Figure 1, but with the crystal oscillator off. Set the step attenuator to maximum attenuation. Set the receiver for SSB or CW reception with its narrowest available IF filter selected. Switch out any internal preamplifiers or RF attenuators. Select AGC off, maximum AF and RF gain. It may be necessary to reduce the AF gain to ensure the audio amplifier is at least 10 dB below its clipping point. The ac voltmeter or an oscilloscope on the AF output can be used to monitor this.

2. To measure noise, it is important to know the bandwidth being measured. A true-RMS ac voltmeter measures the power in the noise reaching it. To calculate the noise density, we need to divide by the receiver's *noise bandwidth*. The receiver's –6-dB IF bandwidth can be used as an approximation, but purists will want to plot the top 20 dB of the receiver's bandwidth on linear scales and integrate the area under it to find the width of a rectangle of equal area and equal height. This accounts properly for the noise in the skirt regions of the overall selectivity. (The very rectangular shape of common receiver filters tends to minimize the error of just taking the approximation.)

Switch on the test oscillator and set the attenuators to give an AF output above the noise floor and below the clipping level with the receiver peaked on the signal. Tune the receiver off to each side to find the frequencies at which the AF voltage is half that at the peak. The difference between these is the receiver's –6-dB bandwidth. High accuracy is not needed: 25% error in the receiver bandwidth will only cause a 1-dB error in the final result. The receiver's published selectivity specifications will be close enough. The benefit of integration is greater if the receiver has a very rounded, low-ringing or low-order filter.

3. Retune the receiver to the peak. Switch the oscillator off and note the noise-floor voltage. Turn the oscillator back on and adjust the attenuator to give an AF output voltage 1.41 times (3 dB) larger than the noise floor voltage. This means that the noise power and the test signal power at the AF output are equal — a value that's often called the *MDS* (*minimum discernible signal*) of a receiver. Choosing a test-oscillator level at which to do this test involves compromise. Higher levels give more accurate results where the phase noise is high, but limit the lowest level of phase noise that can be measured because better receiver oscillators require a greater input signal to produce enough noise to get the chosen AF-output level. At some point, either we've

taken all the attenuation out and our measurement range is limited by the test oscillator's available power, or we overload the receiver's front end, spoiling the results.

Record the receiver frequency at the peak, (f_0), the attenuator setting (A_0) and the audio output voltage (V_0). These are the carrier measurements against which all the noise measurements will be compared.

4. Now you must choose the offset frequencies — the separations from the carrier — at which you wish to make measurements. The receiver's skirt selectivity will limit how close to the carrier noise measurements can be made. (Any measurements made too close in are valid measurements of the receiver selectivity, but because the signal measured under these conditions is sinusoidal and not noise like, the corrections for noise density and noise bandwidth are not appropriate.) It is difficult to decide where the filter skirt ends and the noise begins, and what corrections to apply in the region of doubt and uncertainty. A good practical approach is to listen to the audio and tune away from the carrier until you can't distinguish a tone in the noise. The ear is superb at spotting sine tones buried in noise, so this criterion, although subjective, errs on the conservative side.

Tune the receiver to a frequency offset from f_0 by your first chosen offset and adjust the attenuators to get an audio output voltage as close as possible to V_0. Record the total attenuation, A_1 and the audio output voltage, V_1. The SSB phase noise (qualified as SSB because we're measuring the phase noise on only one side of the carrier, whereas some other methods cannot segregate between upper and lower noise sidebands and measure their sum, giving DSB phase noise) is now easy to calculate:

$$L(f) = A_1 - A_0 - 10_{\log}(BW_{noise}) \quad (1)$$

where

$L(f)$ = SSB phase noise in dBc/Hz

BW_{noise} = receiver noise bandwidth, Hz

A_0 = Attenuator setting in step three

A_1 = Attenuator setting in step four

This equation begins with the difference between the attenuation necessary to reduce the peak carrier signal to the MDS level (A_0 in step three) and the attenuation necessary to reduce the phase noise to the MDS level (A_1 in step four). Subtracting the bandwidth correction term results in the noise power per Hz of bandwidth with respect to the peak carrier signal. Note that this equation does not depend on the absolute power level of the carrier signal as long as it remains constant during the test.

5. It's important to check for overload. Decrease the attenuation by 3 dB, and record the new audio output voltage, V_2. If all is well, the output voltage should increase by 22% (1.8 dB); if the receiver is operating nonlinearly, the increase will be less. (An 18% increase is still acceptable for the overall accuracy we want.) Record V_2/V_1 as a check: a ratio of 1.22:1 is ideal, and anything less than 1.18:1 indicates a bad measurement.

If too many measurements are bad, you may be overdriving the receiver's AF amplifier, so try reducing the AF gain and starting again back at Step 3. If this doesn't help, reducing the RF gain and starting again at Step 3 should help if the compression is occurring late in the IF stages.

6. Repeat Steps 4 and 5 at all the other offsets you wish to measure. If measurements are made at increments of about half the receiver's bandwidth, any discrete (non-noise) spurs will be found. A noticeable tone in the audio can indicate the presence of one of these. If it is well clear of the noise, the measurement is valid, but the noise bandwidth correction should be ignored, giving a result in dBc.

Table 1 shows the results for an ICOM IC-745 as measured by KI6WX, and **Figure 2** shows this data in graphic form. His oscillator power was only –3 dBm, which limited measurements to offsets less than 200 kHz. More power might have allowed noise measurements to lower levels, although receiver overload places a limit on this. This is not important, because the real area of interest has been thoroughly covered. When attempting phase-noise measurements at large offsets, remember that any front-end selectivity, before the first mixer, will limit the maximum offset at which LO phase-noise measurement is possible.

Table 1
SSB Phase Noise of ICOM IC-745 Receiver Section

Oscillator output power = –3 dBm (0.5 mW)
Receiver bandwidth (Δf) = 1.8 kHz
Audio noise voltage = –0.070 V
Audio reference voltage (V_0) = 0.105 V
Reference attenuation (A_0) = 121 dB

Offset Frequency	*Attenuation (A_1) (dB)*	*Audio V_1 (volts)*	*Audio V_2 (volts)*	*Ratio V_2/V_1*	*SSB Phase Noise (kHz) (dBc/Hz)*
4	35	0.102	0.122	1.20	–119
5	32	0.104	0.120	1.15	–122*
6	30	0.104	0.118	1.13	–124*
8	27	0.100	0.116	1.16	–127*
10	25	0.106	0.122	1.15	–129*
15	21	0.100	0.116	1.16	–133*
20	17	0.102	0.120	1.18	–137
25	14	0.102	0.122	1.20	–140
30	13	0.102	0.122	1.20	–141
40	10	0.104	0.124	1.19	–144
50	8	0.102	0.122	1.20	–146
60	6	0.104	0.124	1.19	–148
80	4	0.102	0.126	1.24	–150
100	3	0.102	0.126	1.24	–151
150	3	0.102	0.124	1.22	–151
200	0	0.104			–154
250	0	0.100			–154
300	0	0.98			–154
400	0	0.96			–154
500	0	0.96			–154
600	0	0.97			–154
800	0	0.96			–154
1000	0	0.96			–154

*Asterisks indicate measurements possibly affected by receiver overload (see text).

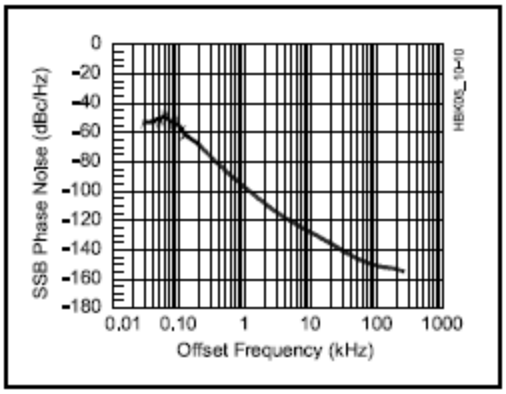


Figure 2 — The SSB phase noise of an ICOM IC-745 transceiver (serial number 01528) as measured by KI6WX.

Measuring Oscillator and Transmitter Phase Noise

Measuring the composite phase noise of a receiver's LO requires a clean test oscillator. Measuring the phase noise of an incoming signal, whether from a single oscillator or an entire transmitter, requires the use of a clean receiver, with lower phase noise than the source under test. The sidebar in the *Handbook's* **Oscillators and Synthesizers** chapter, "Transmitter Phase-Noise Measurement in the ARRL Lab," details the method used to measure composite noise (phase noise and amplitude noise, the practical effects of which are indistinguishable on the air) for *QST* Product Reviews. Although targeted at measuring high power signals from entire transmitters, this approach can be used to measure lower-level signals simply by changing the amount of input attenuation used.

At first, this method — using a low-frequency spectrum analyzer and a low-phase-noise signal source — looks unnecessarily elaborate. A growing number of radio amateurs have acquired good-quality spectrum analyzers for their shacks since older model Tektronix and Hewlett-Packard (now Agilent) instruments have started to appear on the surplus market at affordable prices. The obvious question is, "Why not just use one of these to view the signal and read phase-noise levels directly off the screen?" Reciprocal mixing is the problem.

Very few spectrum analyzers have clean enough local oscillators not to completely swamp the noise being measured. Phase-noise measurements involve the measurement of low-level components very close to a large carrier, and that carrier will mix the noise sidebands of the *analyzer's* LO into its IF. Some way of notching out the carrier is needed, so that the analyzer need only handle the noise sidebands. A crystal filter could be designed to do the job, but this would be expensive, and one would be needed for every different oscillator frequency to be tested. The alternative is to build a direct-conversion receiver using a clean LO like the Hewlett-Packard HP8640B signal generator and spectrum-analyze its "audio" output with an audio analyzer. This scheme mixes the carrier to dc; the LF analyzer is then ac-coupled, and this removes the carrier. The analyzer can be made very sensitive without overload or reciprocal mixing being a problem.

The remaining problem is then keeping the LO — the HP8640B in this example — at exactly the carrier frequency. 8640s are based on a shortened-UHF-cavity oscillator and can drift a little. The oscillator under test will also drift. The task is therefore to make the 8640B track the oscillator under test. For once we get something for free: The HP8640B's FM input is dc coupled, and we can use this as an electronic fine-tuning input. As a further bonus, the 8640B's FM deviation control acts as a sensitivity control for this input. We also get a phase detector for free, as the mixer output's dc component depends on the phase relationship between the 8640B and the signal under test (remember to use the dc coupled port of a diode ring mixer as the output). Taken together, the system includes everything needed to create a crude phase-locked loop that will automatically track the input signal over a small frequency range. **Figure 3** shows the arrangement.

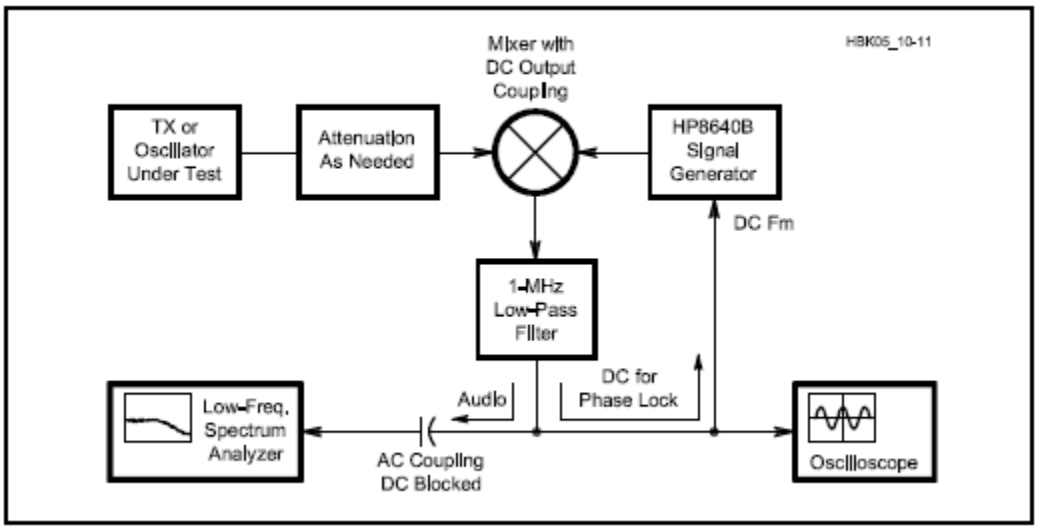


Figure 3 — Arrangement for measuring phase noise by directly converting the signal under test to audio. The spectrum analyzer views the signal's noise sidebands as audio; the signal's carrier, converted to dc, provides a feedback signal to phase-lock the Hewlett-Packard HP8640B signal generator to the signal under test.

The oscilloscope is not essential for operation, but it is needed to adjust the system. With the loop unlocked (8640B FM input disconnected), tune the 8640 off the signal frequency to give a beat at the mixer output. Adjust the mixer drive levels to get an undistorted sine wave on the scope. This ensures that the mixer is not being overdriven. While the loop is off-tuned, adjust the beat to a frequency within the range of the LF spectrum analyzer and use it to measure its level, "A_c" in dBm. This represents the carrier level and is used as the reference for the noise measurements. Connect the FM input of the signal generator, and switch on the generator's dc FM facility. Try a deviation range of 10 kHz to start with. When you tune the signal generator toward the input frequency, the scope will show the falling beat frequency until the loop jumps into lock. Then it will display a noisy dc level. Fine tune to get a mean level of 0 V. (This is a very-low-bandwidth, very-low-gain loop. Stability is not a problem; careful loop design is not needed. We actually want as slow a loop as possible; otherwise, the loop would track and cancel the slow components of the incoming signal's phase noise, preventing their measurement.)

When you first take phase-noise plots, it's a good idea to duplicate them at the generator's next lower FM-deviation range and check for any differences in the noise level in the areas of interest. Reduce the FM deviation range until you find no further improvement. Insufficient FM deviation range makes the loop's lock range narrow, reducing the amount of drift it can compensate. (It's sometimes necessary to keep gently trimming the generator's fine tune control.)

Set up the LF analyzer to show the noise. A sensitive range and 100-Hz resolution bandwidth are appropriate. Measure the noise level, "A_n" in dBm. We must now calculate the noise density

that this represents. Spectrum-analyzer filters are normally *Gaussian*-shaped and bandwidth-specified at their –3-dB points. To avoid using integration to find their true-noise power bandwidth, we can reasonably assume a value of 1.2 × BW. A spectrum analyzer logarithmically compresses its IF signal ahead of the detectors and averaging filter. This affects the statistical distribution of noise voltage and causes the analyzer to read low by 2.5 dB. To produce the same scale as the ARRL Lab photographs prior to May 2006 *QST*, the analyzer reference level must be set to –60 dBc/Hz, which can be calculated as:

$$A_{ref} = A_c - 10 \log (1.2 \times BW) + 62.5 \text{ dBm} \quad (2)$$

where

A_{ref} = analyzer reference level, dBm
A_c = carrier amplitude, dBm

This produces a scale of –60 dBc/Hz at the top of the screen, falling to –140 dBc/Hz at the bottom. The frequency scale is 0 to 20 kHz with a resolution bandwidth (BW in the above equation) of 100 Hz. This method combines the power of *both* sidebands and so measures DSB phase noise. To calculate the equivalent SSB phase noise, subtract 3 dB for non-coherent noise (the general "hash" of phase noise) and subtract 6 dB for coherent, discrete components (that is, single-frequency spurs). This can be done by setting the reference level 3 to 6 dB higher.

Low-Cost Phase Noise Testing

All that expensive equipment may seem far beyond the means of the average Amateur Radio experimenter. With careful shopping and a little more effort, alternative equipment can be put together for pocket money. (All of the things needed — parts for a VXO, a surplus spectrum analyzer and so on — have been seen on sale cheap enough to total less than $100.) The HP8640B is good and versatile, but for use at one oscillator frequency, you can build a VXO for a few dollars. It will only cover one oscillator frequency, but a VXO can provide even better phase-noise performance than the 8640B. There is free software available so that you can use your PC soundcard as an LF spectrum analyzer, though you may want to add a simple preamp and some switched attenuators.

Pontius has also demonstrated that signal-source phase-noise measurements can be accurately obtained without the aid of expensive equipment. (B. E. Pontius, "Measurement of Signal Source Phase Noise with Low-Cost Equipment," *QEX*, May-Jun 1998, pp 38-49.)

Ulrich L. Rohde, Phd, N1UL

A Novel Grounded Base Oscillator Design for VHF/UHF Frequencies

Introduction:

The design of VHF/UHF oscillators has been described in many books and journals. Most of the emphasis was on frequency stability and to some smaller part on output/efficiency. Since the introduction of reliable Phase noise measurements and the ability to predict/simulate the phase noise, the improvement of this important parameter with the help of CAD and analytic equations has gained more attention. The vast majority of early publications focused on designs using small signal approaches which give non-reliable answers for output frequency, output power and phase noise. The purpose of this paper is to validate the large signal time domain approach using the grounded base oscillator rather than the Colpitts oscillator. The key contributions are: (1) to predict the phase noise correctly using the large signal time domain calculations (Bessel functions) and nonlinear CAD simulators and derive a set of algebraic equations for the noise calculations (many of the CAD tools give incorrect answers about the phase noise) and (2) to give set of empirical equations to guide the synthesis of such an "optimized" oscillators. This novel design concept using a time domain approach provides both the best output power and the best phase noise.
To have a point of reference the traditional small signal approach is first used followed by the novel approach shown here to get the optimum design. Using a mix of linear equations and one large signal parameter (gm), the important noise parameters are calculated and validated. Finally, based on this, a very simple but powerfully scalable set of formulas for the oscillator synthesis is shown, that provides extremely good results. In addition to this, the design principle for fixed or narrowband oscillator discussed here also applies to the broadband VCO design. We have shown that even multi-octave band (1:3 frequency tuning range) works well with this design methodology [20-23].

1. Reference circuit:

A very popular circuit for VHF/UHF oscillators is the grounded base configuration, which his shown in figure 1. Its phase noise can be made very good, since the RF voltage swing at the collector can be close to the supply voltage. The circuit is simple and has been used for decades. The oscillator function is based on the principle that power from the output is taken and fed to the emitter. This feedback arrangement generates a negative resistance at the output, compensating the losses of the output-tuned circuit, and starts oscillating and then stabilizing the oscillation amplitude [1,2,3,4]. A complete survey of configurations and applications is found in [5 to 19].

Several books on the topic of Oscillators have been published in the recent years. The references quoted above give a list of the most popular ones. Many of the authors have attempted to predict the oscillators performance based on a set of linear calculation including using the Leeson model or similar methods to determine the phase noise. The problem there is that there are important input parameters required such as the large signal noise figure of the transistor, output power and operating Q. They are typically guessed, but not known. The first successful attempt to determine the large signal phase noise was done by [6, 7].

But these approaches were not useful without a CAD tool and don't give any design guides. Another interesting phenomenon that has been overlooked by the linear approach is that prediction of the exact Oscillator frequency that can be far off compared to the actual frequency of Oscillation.

The recent book by Gonzalez [8] gives an interesting overview of designing Oscillators using linear calculations and CAD, but his design does not provide the optimum solution. To demonstrate this we are going to first use his way to design a 144 MHz Oscillator. The resulting circuit neither gives the best out put power nor the best phase noise and, at high frequencies, requires values for the capacitors, which cannot be easily realized because of parasitic effects.

Figure 1 shows the typical configuration of the grounded base oscillator circuit.

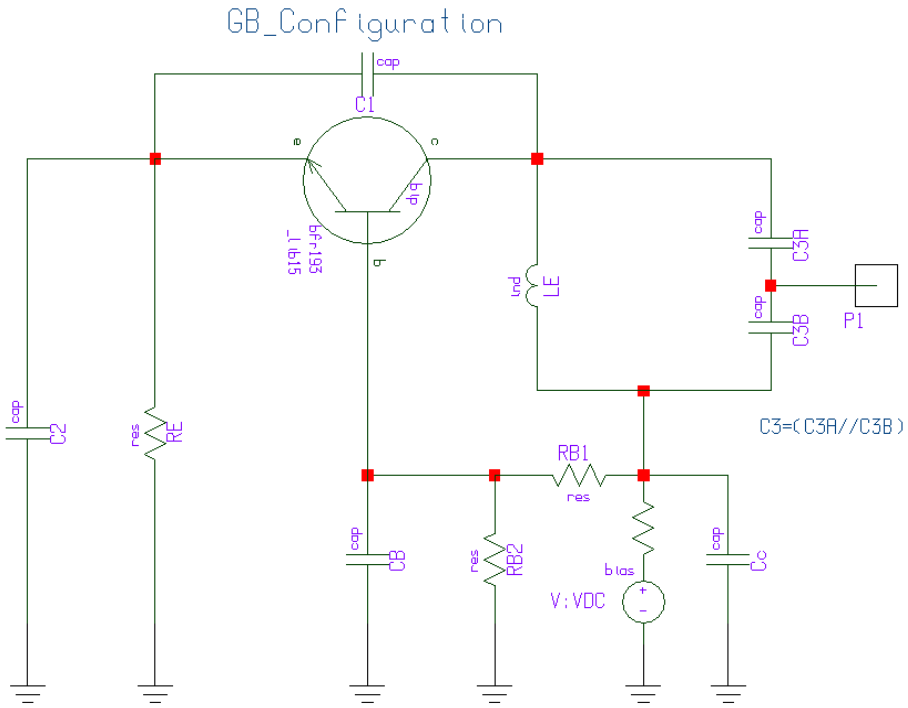


Figure 1 Typical configuration of grounded base oscillator circuit

This oscillator type works well from RF frequencies like 10 MHz to above 1000 MHz. We will now follow [8]. For large signal conditions see Ref [11]. Kenneth Clarke was probably the first to publish the effect of the collector current conducting angle of an oscillator, but makes no mentioning of the relationship of it on the phase noise, which is done on [10].

The [Y] parameters

The first step is to determine the small signal [Y] parameters for the transistor BFR 193 (Infineon), at the frequency of 144MHz, and the operating point: I_c=10mA, I_B=24µA, V_{be}=0.64V, Vce=8.8 V
The 10 mA operating point was selected for a stable transistor cut-off frequency f_T. For more output power 30 mA is a better choice.

Figure 2 shows the circuit generating the small signal [Y] parameters using the Ansoft Designer CAD and the time domain model.

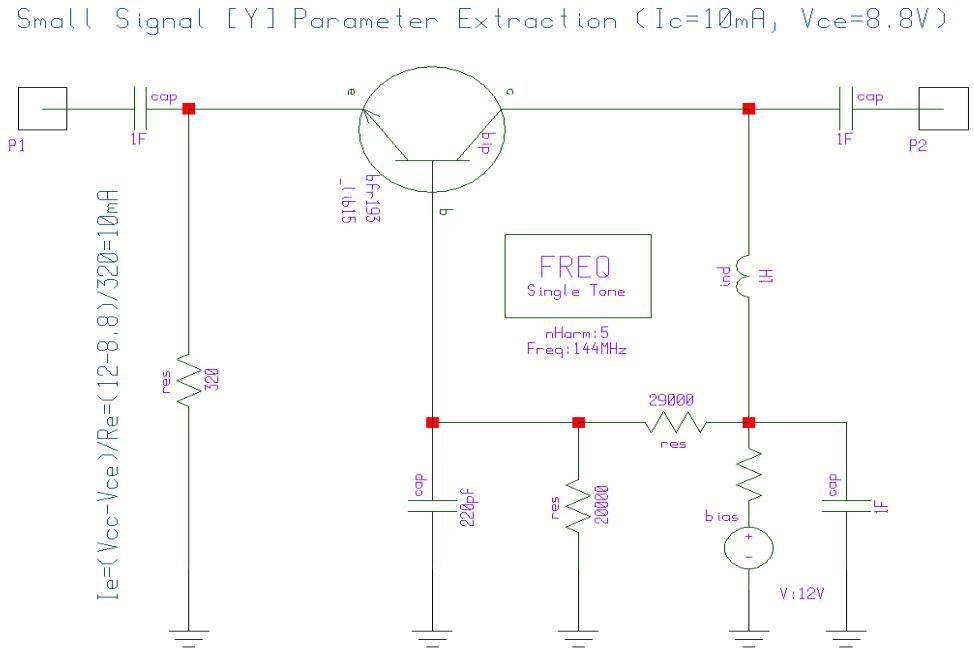
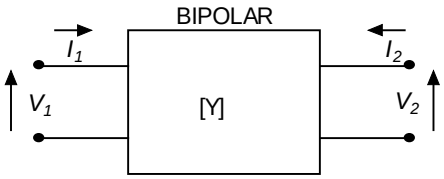


Fig.2. Small signal Y parameter generating circuit with CAD using Infineon time domain model

Based on the following definition:



$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

the CAD software generates the Y-parameters.

We obtain:

$$Y_{11} = G_{11} + jB_{11} = (279.08 - j95.07)\ mS$$

$$Y_{21} = G_{21} + jB_{21} = (-271.32 + j100.77)\,mS$$

$$Y_{12} = G_{12} + jB_{12} = (-1030 + j78.06)\ \mu S$$

$$Y_{22} = G_{22} + jB_{22} = (1020 + j536.14)\ \mu S$$

Parallel Feedback Oscillator Toplogy

The feedback arrangement shown in Figure 3 is the standard feedback Oscillator topology using parallel elements. Theoretically the grounded base configuration can be rotated to be the Colpitts circuit. This statement is often found in the literature [5]. It is based on the black box theory. If we look at the performance, it is not correct that a mathematical rotation yields the same performance. In the case of the Colpitts Oscillator the RF voltage swing is now limited by the base emitter and emitter to ground voltage and as a result there is less energy stored in the circuit and because of loading the operational *Q* can be less than in the grounded base configuration. Here V_{cb} is about 12 volts. Also Y_{22cb} is less than Y_{22ce}, resulting less loading. The Colpitts Oscillator is popular because of its simplicity, and its perceived high isolation as the output power is taken at the collector. However, due to the strong Miller effect at very high frequencies, this is not a true statement. These comments set aside the general approach in the time domain shown here is valid not only for the Colpitts Oscillator but other derivatives.

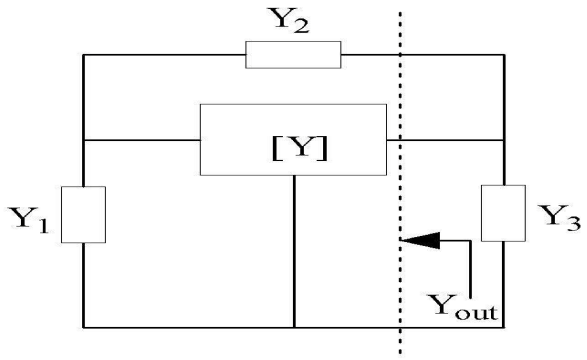


Figure 3. Parallel feedback oscillator topology

The necessary oscillation condition for the parallel feedback oscillators as shown in Figure 3 can be described by

$$Y_{out} + Y_3 \Rightarrow 0$$

This condition can be expressed as

$$Det\begin{bmatrix} Y_{11} + Y_1 + Y_2 & Y_{12} - Y_2 \\ Y_{21} - Y_2 & Y_{22} + Y_2 + Y_3 \end{bmatrix} = 0$$

$$Y_3 = -[Y_{22} + Y_2] + \frac{[Y_{12} - Y_2][Y_{21} - Y_2]}{[Y_{11} + Y_1 + Y_2]}$$

where Y_{ij} (i,j=1,2) are the small signal [Y] parameters of the bipolar or FET model.

Calculation of the feedback network values [linear case]:

As shown in Figure 3, the active 2-port network, together with the feedback elements Y_1 and Y_2, are considered as a one-port negative resistance oscillator circuit. The following is an example of an Oscillator design using the small signal parameter determined above at 8.8 Volts and 10 mA at 144 MHz. The output admittance Y_{out} is

$$Y_{out} = -Y_3 \Rightarrow [Y_{22} + Y_2] - \frac{[Y_{12} - Y_2][Y_{21} - Y_2]}{[Y_{11} + Y_1 + Y_2]}$$

The optimum values of feedback element are calculated from the expression of B_1^* and B_2^*, and for 10 mA are:

$$B_1^* = -\left\{ B_{11} + \left[\frac{B_{12} + B_{21}}{2} \right] + \left[\frac{G_{21} - G_{12}}{B_{21} - B_{12}} \right] \left[\frac{G_{12} + G_{21}}{2} + G_{11} \right] \right\}$$

$$jB_1^* = j\omega C_1$$

$$C_1 \cong 478\,pF$$

$$B_2^* \cong 417 \times 10^{-3}$$

$$jB_2^* = j\omega C_2$$

$$C_2 \cong 459\,pF$$

The optimum values of the real and imaginary part of the output admittance are

$$Y_{out}^* = [G_{out}^* + jB_{out}^*]$$

where G_{out}^* and B_{out}^* are values for conjugate matching!

$$G_{out}^* = G_{22} - \left[\frac{(G_{12} + G_{21})^2 + (B_{21} - B_{12})^2}{4G_{11}} \right]$$

$$G_{out}^* \approx -74.5 \times 10^{-3}$$

needed to compensate the resonator losses ,

$$B_{out}^* = B_{22} + \left[\frac{G_{21} - G_{12}}{B_{21} - B_{12}} \right] \left[\frac{(G_{12} + G_{21})}{2} + G_{22} - G_{out}^* \right] + \left[\frac{B_{21} + B_{12}}{2} \right]$$

$$B_{out}^{*} \approx 214.74 \times 10^{-3}$$

$$C_3 \approx 237\,pF$$

$$\omega_0 = \frac{1}{2\pi\sqrt{LC}}; \quad C \approx 471 pF$$

$$For \quad f_0 = 144 MHz, \quad L_3 \approx 2.59 nH$$

Figure 4 shows the 144MHz oscillator circuit using the small signal Y parameter for establishing oscillation conditions. The required values for this parallel feedback topology are: 478 pF for the feedback capacitor, 459 pF for the emitter to ground, the inductor 3.2 nH, and 186 pF for C3A and C3B. The bypass capacitors C_b and C_c should be about 220 pF.

However, it is practically impossible to manufacture capacitors above 200 pF to be capacitive at these frequencies. The best but awkward method then is to use a few capacitors in parallel

And for 30 mA:

$$Y_{11} = G_{11} + jB_{11} = (437 - j295)\ mS$$
$$Y_{21} = G_{21} + jB_{21} = (-427 + j296)\,mS$$
$$Y_{12} = G_{12} + jB_{12} = (-1670 + j757)\ \mu S$$
$$Y_{22} = G_{22} + jB_{22} = (1650 - j146)\ \mu S$$

For f_0= 144 MHz and 30mA, the component values are: L=3.77 nH, C_1=518 pF, C_2=503 pF, C_3=69 pF, C=324 pF, needless to say C_1 and C_2 are paralleled capacitors in the vicinity of 100 pF each.

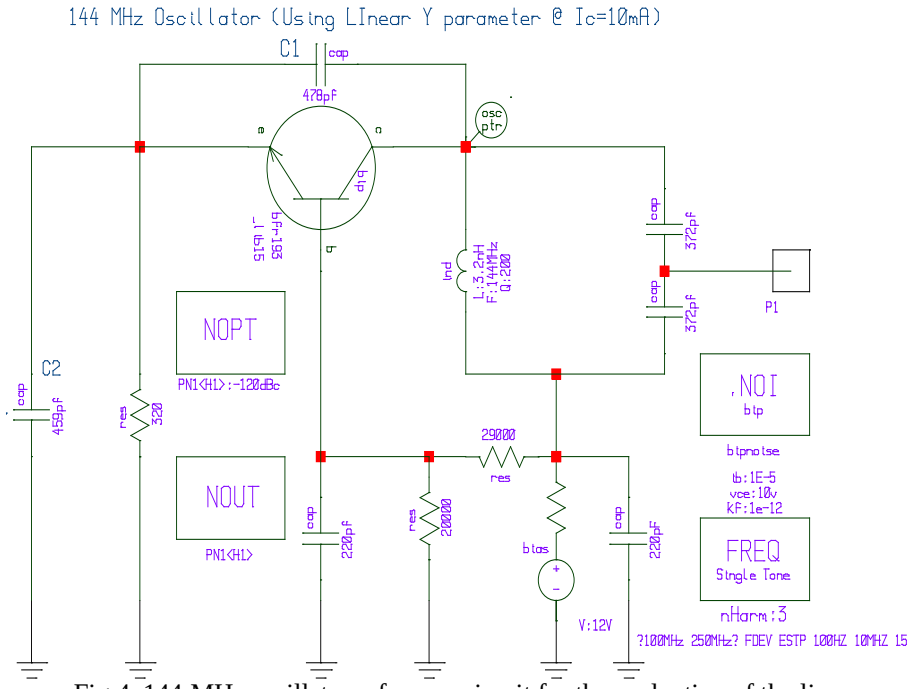


Fig 4. 144 MHz oscillator reference circuit for the evaluation of the linear approach

Figures 5 shows the simulated plot of the phase noise. The “linear “calculation indicates a resonant frequency of 143.2 MHz, while the non-linear harmonic balance (HB) analysis supplies the correct frequency of 144.2 MHz (quite a difference in percent) and an output power of (only) 5.1 dBm, as seen in Fig 6. This value is determined using the HB programs Ansoft Designer (Nexxim). ADS give the same answer. These CAD tools deviate less then 1 dB from measured results, if the input Spice type parameters for the transistor are accurate.

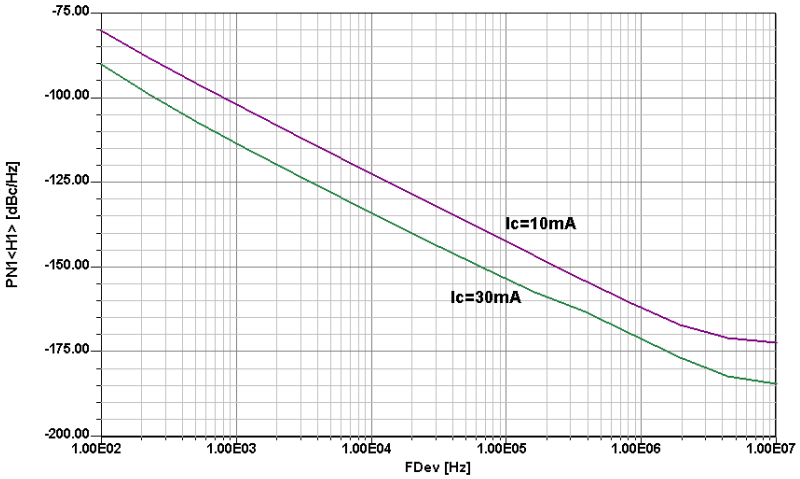


Fig 5. Phase noise plot of 144 MHz oscillator reference circuit for the evaluation of the **linear** approach (both 10 mA and 30 mA case). The 30 mA case gives 10dB lower phase noise than 10 mA case.

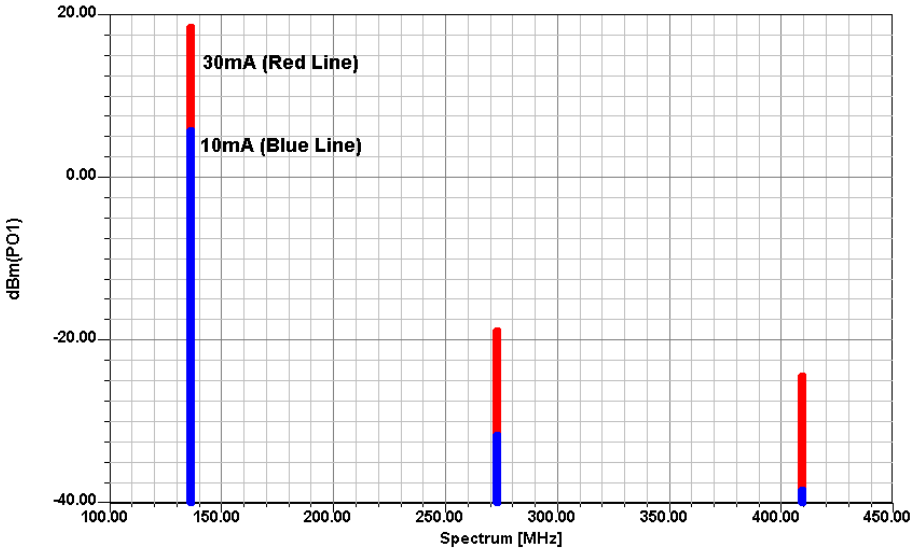


Fig 6. RF output power of 144 MHz oscillator reference circuit for the evaluation of the linear approach Both 10 mA and 30 mA are shown. For 30 mA, 12dB more power is available, now a total of approximately 18 dBm.

Large Signal and Noise Analysis

There were a variety of efforts made to deal with the large signal conditions, like the time domain approach. Reference [10] is a first successful attempt to deal with the calculations of the output power with reasonable effort. See Eq. (10) of this publication. There are many problems associated with both the large signal analysis as well as the noise analysis. From an experimentally point of view it is partially impossible to build all possible variations. So we were trying to determine if the Ansoft Designer, whose large signal noise analysis development we were involved with, would give us the correct prediction. We were aware that all researchers would primarily look for measured data (which we will show) and yet we had to convince them that our CAD tool was reliable. Therefore we took a few critical circuits, running from Crystal Oscillators to VCO's and evaluated them again. These were available during the development of the Designer CAD tool, and we re-measured them, with more refined test equipment like the R&S FSUP 26 and its necessary options. In [12,13] we have shown that the accuracy of the prediction was within 0.5dB of the measured results. During this effort to analyze the noise in oscillators with a set of equation using a minimum of expensive CAD tools, we found this was possible. These equations, derived in [9], will be used here.

A Novel Approach using the time-domain analysis for obtaining the best phase noise and output power.

The hunt for a combined low phase noise can be followed through the literature. Designers have published recipes, like the use of low noise transistors, high Q circuit, and other things, but the consequences of the large signal operation and the resulting phase noise had not been fully understood. A complete mathematical treatment follows for a 144 MHz oscillator.

Design Steps

1) Calculation of the output power for the selected DC operating conditions:
We select the same circuit as above, and set f_o = 144 MHz.
From [9], the RF output current is:

$$I_{RF}(t) = I_c(t) \cong I_e(t) = I_{dc}\left[1 + 2\sum_{1}^{\infty}\frac{I_n(x)}{I_0(x)}\cos(n\omega t)\right] = 10\times10^{-3}[1+6.6]_{x=15} \Rightarrow I_{RF}(t) = 60mA\,(Peak-Amplitude)$$

$$where\ x\ is\ normalized\ drive\ level \quad (x = \frac{qV_1}{kT};\ V_1 = Drive\ signal)$$

Considering 50 Ω load, the RF output power is calculated:

$$V_{RF}(f_0) = I_{RF}\times 50 = 60\times10^{-3}\times 50 = 1\,Volt\ (Peak-Amplitude) \qquad \text{(No Vce saturation assumed!)}$$

The oscillator output power at 144 MHz is then

$$P_{out}(f_0) = \frac{V_{RF}^2(f_0)}{2R_L} = \frac{1}{2\times 50} = 10mW = 10dBm$$

2) Calculation of the large signal transconductance for the normalized drive level x=15.

$$Y_{21}\big|_{small-signal} = \frac{I_{dc}}{kT/q} = \frac{I_{dc}}{V_T} = g_m \Rightarrow g_m = \frac{3\times10^{-3}}{26mV} \approx 115mS \quad (k = Boltzman\ conctsnat, T = 298\ K)$$

The large signal transconductance G_m is now

$$Y_{21}\big|_{large-signal} = G_m(x) = \frac{qI_{dc}}{kTx}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} = \frac{g_m}{x}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} \approx 20mS\ (for\ x \approx 15)$$

This assumes an ideal intrinsic transistor. To perform the transition from the intrinsic to extrinsic transistor, we add the parasitics (package effects, lead inductance and bond wires) by correcting the final results for capacitances and inductances. The f_t of the transistor used is high enough so a phase shift correction for g_m is not necessary at this frequencies (VHF).

3) Calculation of the feedback capacitors:

The value of n can be in the range of n [n_1, n_2], where n_1 is 2 and n_2 is 5 for a drive level x=15 (low phase noise performance!!!).

Assume n =5, the values of C_1 and C_2 can be calculated to be

$$\frac{C_2}{C_1 + C_2} = \frac{1}{n} \Rightarrow C_2 = \frac{C_1}{n-1}$$

$$C_2 = \frac{C_1}{n-1} = \frac{C_1}{4} \Rightarrow \frac{C_1}{C_2} = 4$$

The ratio of the capacitor C_1 to C_2 is 4.

4) Calculation of the component values (C_1, C_2, C_3, C_4, and L)

(a) Calculation of C_1 and C_2

The value of C_1 is selected for proper loading, therefore

$$XC_1 > Y_{11} \approx C_1 > \frac{Y_{11}}{\omega} \Rightarrow C_1 > \frac{Y_{21}}{\omega} \cong C_1 \geq \frac{2G_m(x)}{\omega} \Rightarrow C_1 > \frac{2 \times 20 \times 10^{-3}}{2 \times 3.1414 \times 144 \times 10^6} \approx 44\,pF$$

For C_1/C_2 =4, $C_2 \cong 11\ pF$

(b) Calculation of C_3 and C_4

For optimum phase noise and power output,

$C_3 \geq 2C_2 \Rightarrow C_3 = 22\,pF$,

and the capacitive transformer tapping ratio m (C_3/C_4) should be greater than 10, therefore the impedance transformation is >100. For C_3 =22 pF, C_4 is 220 pF.

(c) Calculation of L

$$\omega_0 = \frac{1}{2\pi\sqrt{LC}}; \quad C = C_T + C_3; \quad C_T = \frac{C_1 \times C_2}{C_1 + C_2} \Rightarrow C \approx 30\,pF$$

$$For \quad f_0 = 144MHz, \quad L_3 = \frac{1}{(2\pi \times 144 \times 10^6)^2 \times 29 \times 10^{-12}} \approx 39nH$$

4) Calculation of the [L/C] ratio:

The energy stored across the resonator circuit for a given conduction angle and drive level is dependent on the characteristic impedance, $Z_0 = \sqrt{\frac{L(nH)}{C(pf)}} \Rightarrow Z_0^2 = 1000\sqrt{\frac{L}{C}} \Rightarrow Z_0 = \sqrt{1200}$

For optimum phase noise and output power, Z should be greater than 3, e.g.
For example, the L/C ratio for a good approach is

$$\frac{L_3}{C_3} = \frac{39 \times 10^{-9}}{30 \times 10^{-10}} = 13 \Rightarrow p > 10$$

Validation

We now use the same test circuit and apply the "new" component values just calculated.

Phase Noise Calculation:

In Reference [9] we have shown the Phase noise calculations for the Colpitts Oscillator. These calculations can also be used to get the Phase noise of this circuit. It agrees well with both measurements and simulations using the Harmonic balance simulator Ansoft Designer (Nexxim).

The individual phase noise contribution can be described by [9]

$$PN_{inr}(\omega_0 + \Delta\omega) = \frac{4KT}{R_P}\left[NFT_{inr}(\omega_0)\right]^2 = \frac{4KT}{R_P}\left\{\frac{1}{2}\left[\frac{1}{2j\omega_0 C_{eff}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow \text{Phase noise}$$

contribution from the resonator tank.

$$PN_{Vbn}(\omega_0 + \Delta\omega) = 4KTr_b\left[NFT_{Vbn}(\omega_0)\right]^2 = 4KTr_b\left\{\frac{1}{2}\left[\frac{C_1 + C_2}{C_2}\right]\left[\frac{1}{2jQ}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow \text{Phase noise}$$

contribution from the base resistance.

$$PN_{ibn}(\omega_0 + \Delta\omega) = 2qI_b\left[NFT_{ibn}(\omega_0)\right]^2 = 2qI_b\left\{\frac{1}{2}\left[\frac{C_2}{C_1 + C_2}\right]\left[\frac{1}{j\omega_0 QC_{eff}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow \text{Phase noise}$$

contribution from the base current.

$$PN_{ifn}(\omega_0 + \Delta\omega) = \frac{K_f I_b^{AF}}{f_m}\left[NF_{ibn}(\omega_0)\right]^2 = \frac{K_f I_b^{AF}}{f_m}\left\{\frac{1}{2}\left[\frac{C_2}{C_1 + C_2}\right]\left[\frac{1}{j2\omega_0 QC_{eff}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow \text{Phase}$$

noise contribution from the flicker noise of the transistor.

$$PN_{icn}(\omega_0+\Delta\omega)=2qI_c\left[NFT_{icn}(\omega_0)\right]^2=2qI_c\left\{\frac{1}{2}\left[\frac{C_1}{C_1+C_2}\right]\left[\frac{1}{2j\omega_0 QC_{eff}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow \text{Phase noise}$$

contribution from the collector current.

The total effect of all the four noise sources can be expressed as

$$PN(\omega_0+\Delta\omega)=[PN_{inr}(\omega_0+\omega)]+[PN_{Vbn}(\omega_0+\omega)]+[PN_{ibn}(\omega_0+\omega)]+[PN_{icn}(\omega_0+\omega)]$$

$$PN(\omega_0+\Delta\omega)=\frac{4KT}{R_P}\left\{\frac{1}{2}\left[\frac{1}{2j\omega_0 C_{eff}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2+4KTr_b\left\{\frac{1}{2}\left[\frac{C_1+C_2}{C_2}\right]\left[\frac{1}{2jQ}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$$

$$+\left[2qI_b+\frac{2\pi K_f I_b^{AF}}{\Delta\omega}\right]\left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{j2Q\omega_0 C_{eff}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2+2qI_c\left\{\frac{1}{2}\left[\frac{C_1}{C_1+C_2}\right]\left[\frac{1}{2j\omega_0 QC_{eff}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$$

where
K_f = Flicker noise constant
AF = Flicker noise exponent.

$$C_{eff}=C+\frac{C_1C_2}{C_1+C_2}$$

Note: The effect of the loading of the Q of the resonator is calculated by the noise transfer function multiplied with the noise sources.
The phase noise contribution from the different noise sources for the parallel tuned Colpitts oscillator circuit at Δf = 10 kHz from the oscillator frequency f_0 = 144 MHz will now be computed:

Circuit parameters:
Base resistance of transistor r_b = 6.14 ohm.

Parallel loss resistance of the resonator R_P = 7056 Ohm.

Q of the resonator = 200 (Q of the inductor at 144 MHz)
Resonator inductance = 39 nH
Resonator capacitance = 22 pF
Collector current of the transistor I_c = 10 mA
Base current of the transistor I_b = 85 uA.
Flicker noise exponent AF = 2
Flicker noise constant K_f = 1E-7
Feedback factor n = 5.
Phase noise @ 10 KHz:

$$PN_{inr}(\omega_0+10KHz)\approx -134.2dBc/Hz$$
$$PN_{Vbn}(\omega_0+10KHz)\approx -151dBc/Hz$$
$$PN_{(ibn+ifn)}(\omega_0+10KHz)\approx -169.6dBc/Hz$$
$$PN_{icn}(\omega_0+10KHz)\approx -150.6dBc/Hz$$

The total sum of all the four noise sources can be expressed as

$$PN(\omega_0+\Delta\omega)=[PN_{inr}(\omega_0+\omega)]+[PN_{Vbn}(\omega_0+\omega)]+[PN_{ibn}(\omega_0+\omega)]+[PN_{icn}(\omega_0+\omega)]\cong -134.1\,dBc/Hz$$

Note: The noise contribution from the resonator at this offset is the same as the flicker noise contribution from the transistor. For low-Q cases, this can be identified as the flicker corner frequency.

Phase noise @ 100Hz:

$$PN_{inr}(\omega_0+100Hz)\approx -94.2dBc/Hz$$
$$PN_{Vbn}(\omega_0+100Hz)\approx -111dBc/Hz$$
$$PN_{(ibn+ifn)}(\omega_0+100Hz)\approx -124.1dBc/Hz$$
$$PN_{icn}(\omega_0+100Hz)\approx -110.6dBc/Hz$$

The total sum of all the four noise sources can be expressed as

$$PN(\omega_0+\Delta\omega)=[PN_{inr}(\omega_0+\omega)]+[PN_{Vbn}(\omega_0+\omega)]+[PN_{ibn}(\omega_0+\omega)]+[PN_{icn}(\omega_0+\omega)]\cong -94.1\,dBc/Hz$$

It appears that the flicker noise and the noise from the resonator are the limiting factors for the overall phase noise performance of the oscillator circuit.

Figures (7) and (8) show the schematic and layout of the 144 MHz oscillator using time domain parameters at Ic=10 mA.

The oscillator circuit shown in Figure 7 uses a lumped inductor of 39 nH and an unloaded Q of 200 at the operating frequency. Even at theses frequency the layout is quite critical. Figure 8, layout shows an assembly of component where the lead inductances have been kept small. The inductor is a standard off the shelf component.

Figures (9), (10), and (11) show the CAD simulated phase noise plot, the measured phase noise plot, and the simulated output power. The simulated and the validated output power now is 11.55dBm (a 6 dB improvement compared to the linear case), and at 10kHz offset from the carrier frequency, the phase noise has been improved to be –135 dBc/Hz from previously –122 dBc/Hz, a 13 dB improvement.

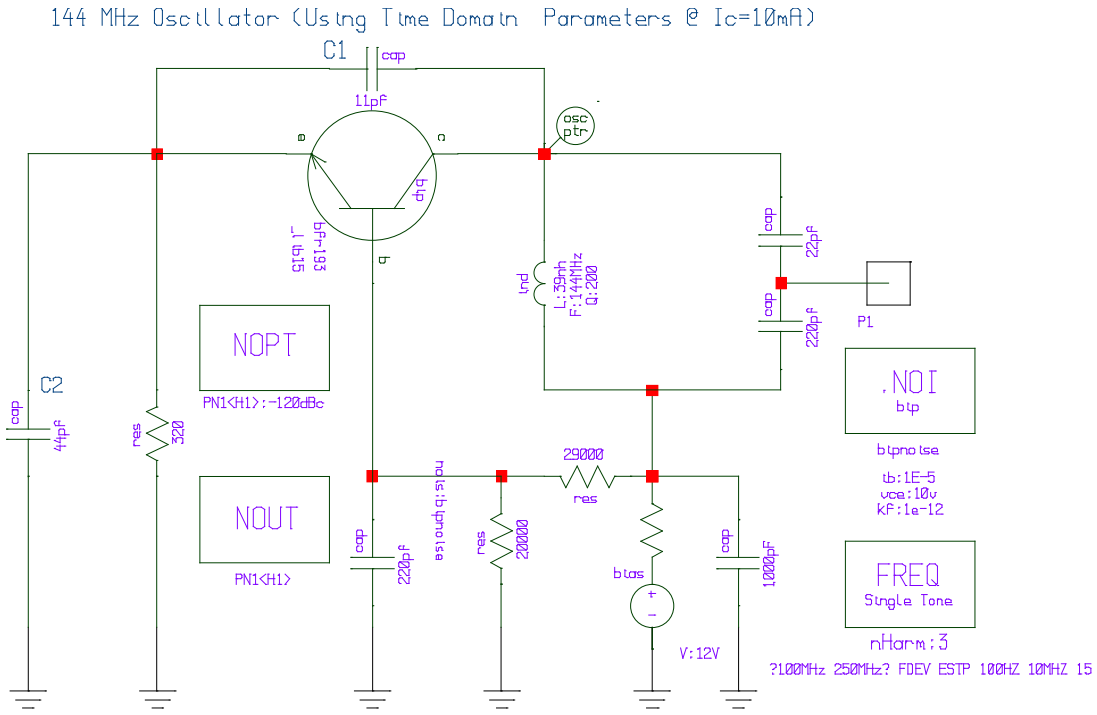


Fig 7. 144 MHz oscillator reference circuit for the evaluation of the time domain approach

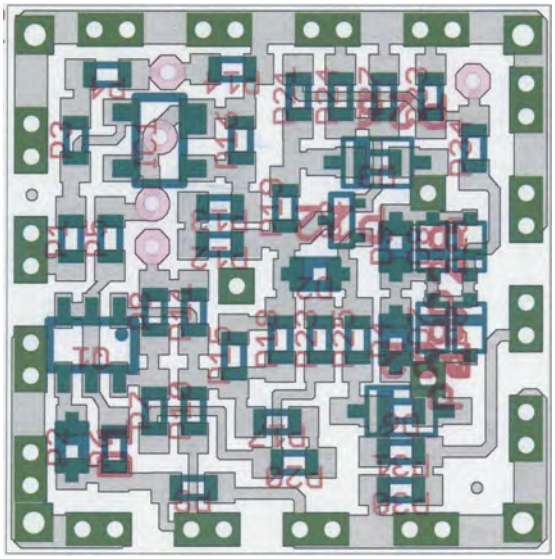


Fig 8 Layout of 144 MHz oscillator circuit using LC lumped inductor capacitor resonator network

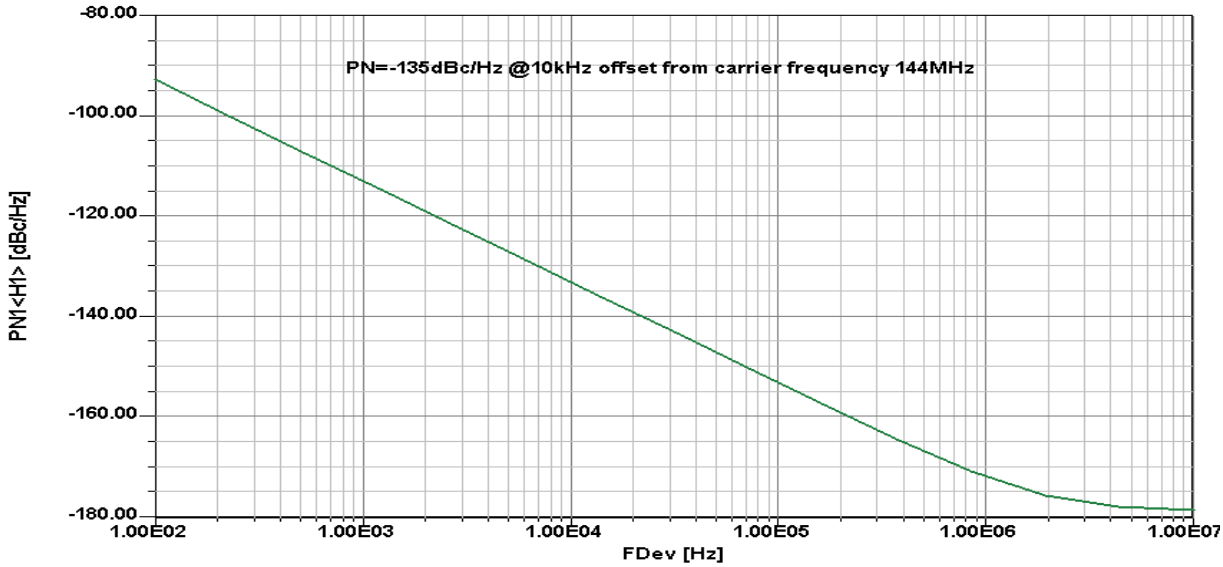


Fig 8. Phase noise plot of 144 MHz oscillator reference circuit for the evaluation of the time domain approach

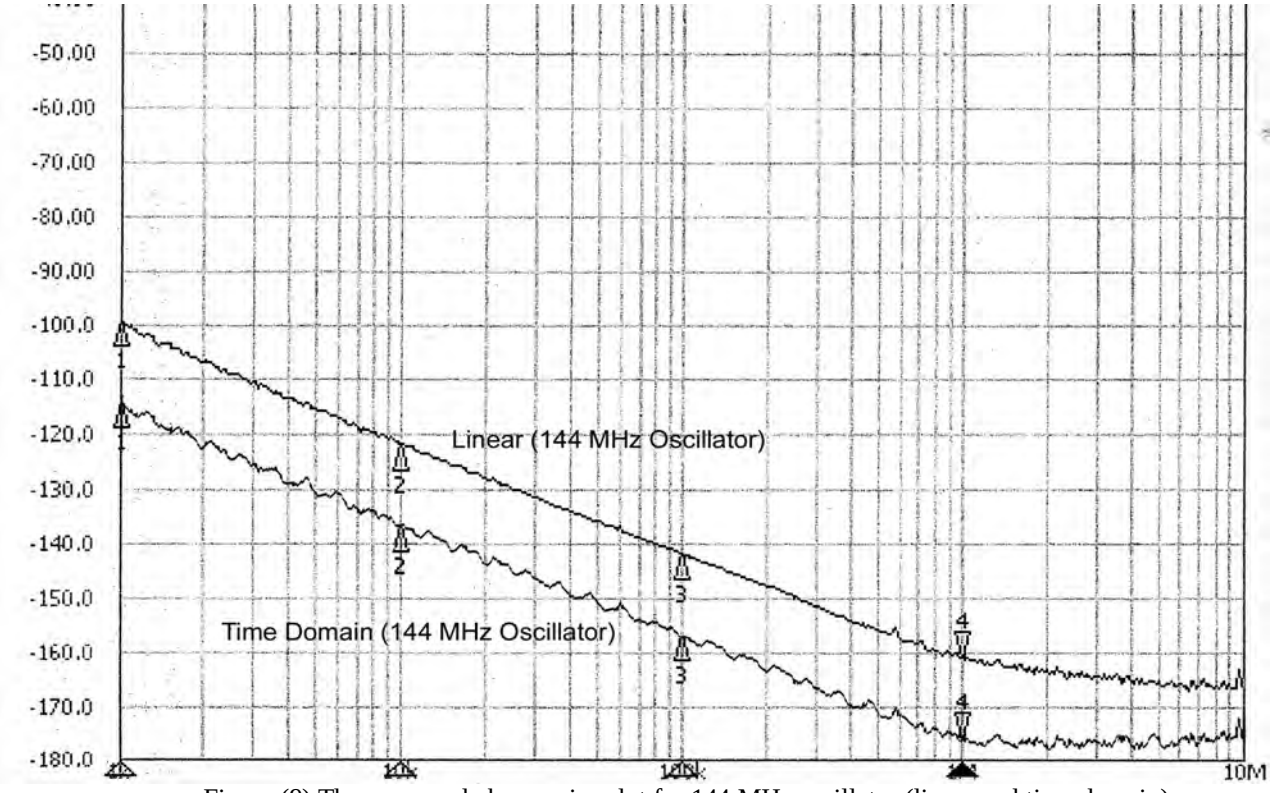


Figure (9) The measured phase noise plot for 144 MHz oscillator (linear and time domain).

Using our phase noise calculation approach as shown above, the result is –134 dBc/Hz and –94 dBc/Hz at 10 kHz and 100 Hz offset. All three results, calculated, simulated, and measured result closely agrees within 1 dB. Many designers may not have access to CAD tools with oscillator noise calculation, and therefore this approach is extremely useful and cost saving.

If we now operate the same transistor at 30 mA, the phase noise at 10 kHz offset will further improved to be –144 dBc/Hz and the output power is increased to 20 dBm. This shows that for low phase noise design a more powerful transistor is a good choice. It is important to keep the DC dissipation of the device in mind, as the CAD approach does not flag a misuse of the device.

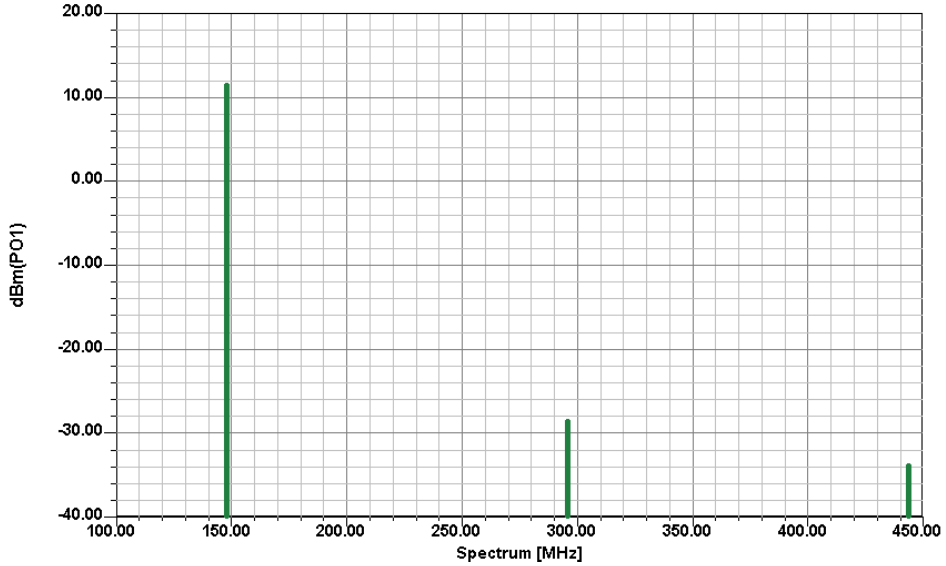


Fig 10. RF output power of 144 MHz oscillator reference circuit for the evaluation of the time domain approach.

Second Example: **433MHz oscillator Circuit:**

Transistor (BFR193 same devices as above), Vce=8.8V, I_c=10 mA, I_B=85μA, V_{be}=0.67V).

Using the same set of equations and design, we now obtain:

$$C_1 = 3.3pF, C_2 = 13pF, C_{3A} = 7.5pF, C_{3B} = 75pF, L_E = 13nH$$
$$R_E = 320\Omega, R_{B1} = 29000\Omega, R_{B2} = 20000\Omega, C_B = 220pF, C_c = 1000pF, V_{DC} = 12V$$

resulting an output power of 11.9 dBm and a phase noise of – 100 dBc/Hz at 10kHz offset from the carrier. Since the 144 MHz was about 35 dB better in the phase noise (– 135 dBc/Hz at 10kHz offset), we need to ask question why? The phase noise and the carrier frequency are related in a quadratic function. This means 3 times increases in frequency results in 9 dB degradation in phase noise for 432 MHz oscillator circuit in comparison to 144 MHz oscillator as shown in Figure 7. Therefore, phase noise performance for 432 MHz oscillator circuit should be – 126 dBc/Hz instead of – 100 dBc/Hz at 10kHz offset (CAD simulated).

The answer is that even in grounded base condition, large signal Re [Y_{22}] loads the parallel tuned circuit significantly resulting in a lower dynamic operating Q. We have to find a work around for this.

The phase noise and the Q are related in a quadratic function. This means 2 times the Q result in 12 dB improvements. Since we lost 26 dB, we need to improve the dynamic loaded operating Q approximately 20 times. As this is not possible, there may be more effects than just the Q deterioration. Here is the answer: “the collector emitter capacitance dynamically detunes the circuit periodically”. A solution for this problem is to tap the inductor, therefore decreasing the influence of the transistor. We will show this now.

Modified Circuit for UHF (432 MHz) and Higher Current

If we inspect Y_{22} of our transistor at 432 MHz and at 30 mA, we will see that the loading of the tank circuit decreases the operating Q significantly. The way around this to apply a center tapped inductor. As the coupling at these frequencies from winding to winding is not extremely high, actually two separate identical inductors can be used successfully.
Figure 11 shows the schematic of 432 MHz grounded base oscillator using the tapped inductor.

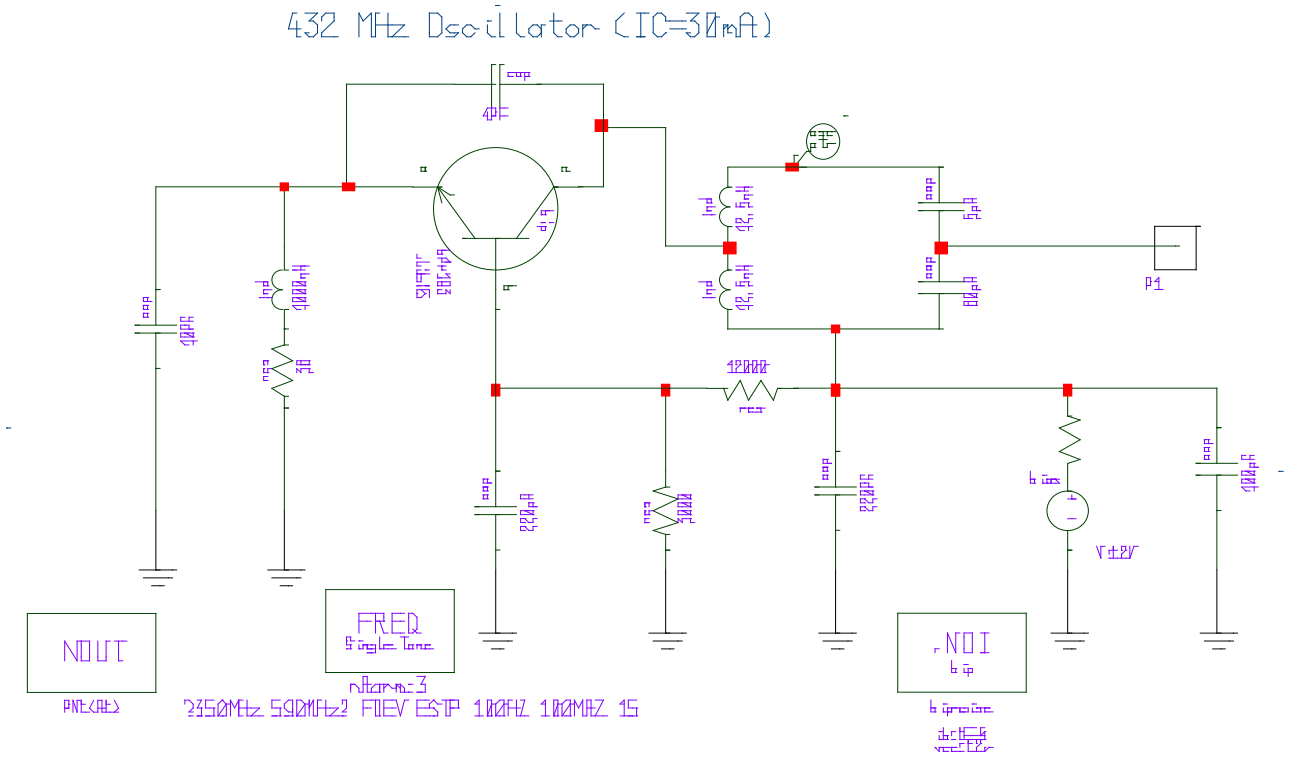


Figure 11 Schematic of 432 MHz grounded base oscillator using tapped inductor (30 mA).

This is a modification of the circuit we have used previously. In the case of a VCO, it would be advantageous to use a different output coupling scheme because in this configuration, the

loading would vary with frequency. This can easily be achieved by adding some inductive coupling to the circuit. In case of a printed resonator this can be accomplished quite simple.

Figure 12 shows the layout of the 433 MHz oscillator circuit using buried printed couple line resonator network (stripline resonator: middle layer).
The actual resonator would not be visible if the oscillator is visually inspected.

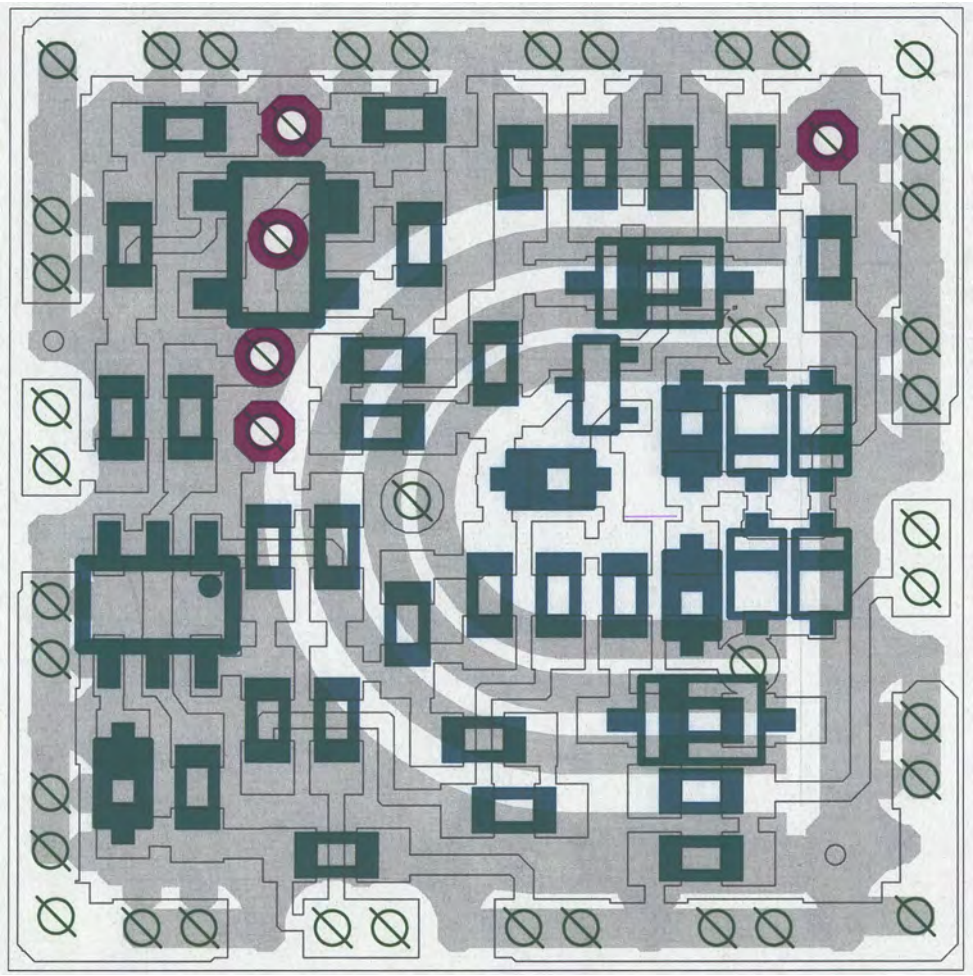


Fig 12. Layout of the 433 MHz oscillator circuit using buried printed couple line resonator network (stripline resonator: middle layer).

Figure 13 shows the simulated phase noise plot. It shows the expected noise degradation of 9 dB, as the frequency is approximately 3 times higher. The resulting simulated output power at 432 MHz is 16 dBm, compared to 18 dBm at 144MHz. This is due to internal package parasitics, which could not be compensated externally. The second harmonic is suppressed by 38 dB; this is due to the higher operating Q.

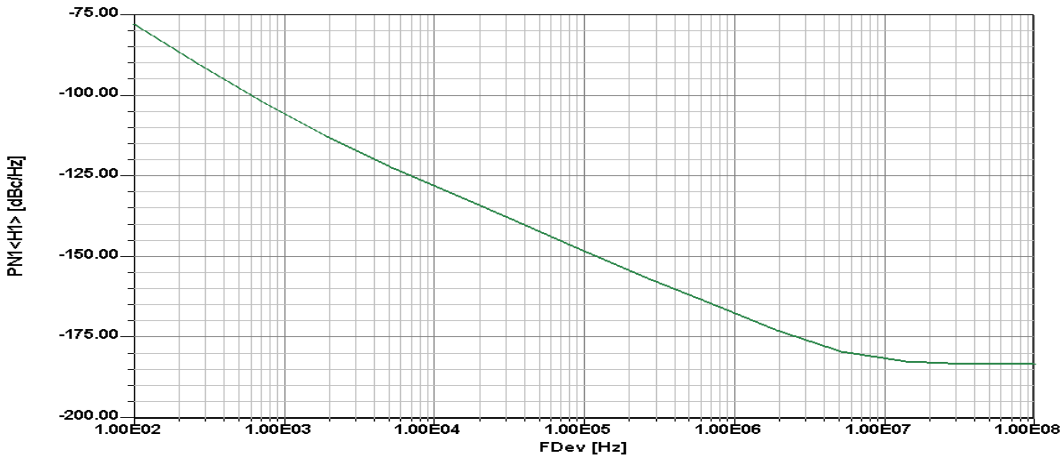


Figure 13. The simulated phase noise plot of 432 MHz grounded base oscillator using tapped inductors

Circuit Design Guidelines:

The results we have obtained so far were based on mathematical calculations. Some of these calculations are difficult to obtain. However, by inspecting the resulting circuits, there are certain relationship between the values of the capacitance of the tuned circuit and the two feedback capacitors, the collector emitter capacitor and the emitter to ground capacitor. The following shows the set of recommended steps for easy design of such oscillator. Figure 14 shows the typical grounded base oscillator for demonstrating the simple design rules where C_E and C_F are the feedback capacitors that generates the negative resistance to compensates the loss resistance of the resonator network comprised of L_E and C_L^*.

Simple Design Rules With an Example:

By setting the L/C ratio to a fixed value of 1200 (this is done for optimum energy storage, group delay and energy transfer for a given cycle in the resonator network), the following should be used:

(1) $$\frac{L}{C} = \left[\frac{L_E}{C_L^*}\right]_{Grounded-Base} = 1200 \Rightarrow Z_0 = \sqrt{1200} \cong 34.6\Omega$$

(2) $$L = 1200 \times C \Rightarrow L_E = 1200 \times C_L^*$$

(3) $$f = \frac{1}{2\pi\sqrt{LC}} \Rightarrow f = \frac{1}{2\pi.C\sqrt{1200}}$$

(4) $$C_L^* = C_L + \frac{C_E C_F}{C_E + C_F}$$; C_E (C_1) and C_F (C_2) are feedback capacitors.

(5) $$C_L = \frac{C_A C_B}{C_A + C_B}$$

(6) $$C_B = 10 \times C_A$$

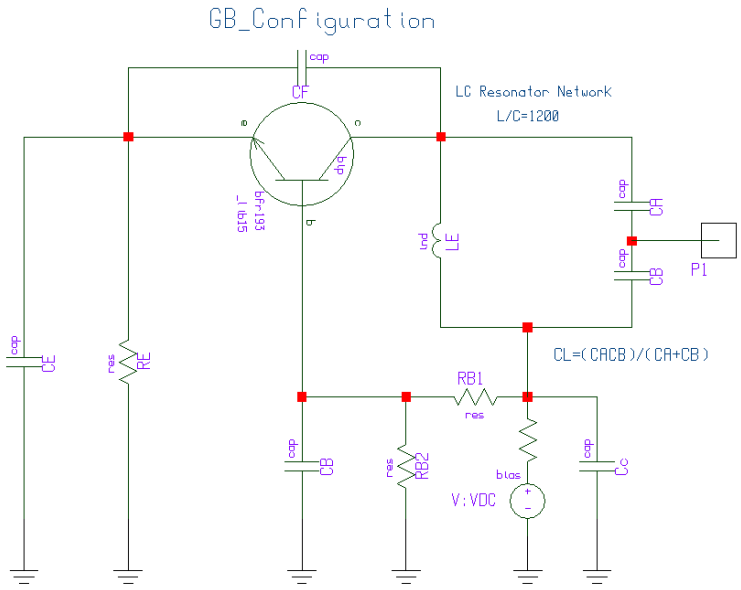


Figure 14 Typical configuration of grounded base oscillator circuit

In order to examine the accuracy of this simple approach, let us take the same 144 MHz grounded base oscillator as shown in Figure 7 (the radio amateur readers will appreciate this).

Example: The 144 MHz Grounded Base Oscillator

$$C_L^* = \frac{1}{2\pi f\sqrt{1200}} \Rightarrow C \cong 31pF$$

$$L_L = \frac{1}{(2\pi f)^2 \times C} \Rightarrow L \cong 39nH$$

$$C_F = 0.3 \times C_L^* \cong 11pF$$

$$C_L = 2 \times C_F \cong 22\,pF$$

$$C_E = 4 \times C_F \cong 44\,pF$$

$$C_A = 22\,pF$$

$$C_B = 220\,pF$$

These results are comparable with the results above and the calculation is frequency scalable with minor corrections possibly, if necessary. Competing other alternative short formulae published in the literature may not deliver the same high performance.

Summary:

Today's applications, both commercial and consumer, require low cost high performance oscillators and the design time is also very critical. The approach shown here meets these requirements and gives detailed guidelines for better performing oscillators. The concept is explained in detail and validated. This is only one of the many applications for which this technique is applicable. Furthermore, by translating this design to integrated circuits very high performance but very low cost oscillators can be made. From a theoretical point, we

found it surprising that simple equations could be found which optimized the design and accurately predicted the phase noise. For the determination of the output power, a nonlinear CAD toll is recommended if the frequencies are higher than 500 MHz. Our example has shown that at frequencies below 200 MHz the output power can be determined quite accurately using this approach.

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A Design Example for an Oscillator for Best Phase Noise and Good Output Power

By Dr. Ulrich Rohde, N1UL

Figure C-1 shows the parallel-tuned Colpitts oscillator circuit, which has to be designed with the following specifications. The unit was also built and measured. It uses a ceramic resonator and its equivalent circuit is shown.

Requirements:

- output power requirement: 13 dBm
- operating frequency: 1000 MHz
- load: 50 Ω
- phase noise –124 dBc/Hz @10KHz

Design Steps

Step 1:

Calculation of the operating point for a fixed, normalized drive of x = 20 (high output power), see Table 6-1.

Based on output power requirement, the following is calculated.

The oscillator output voltage at the fundamental frequency is

$$V_{out}(\omega_0) = \sqrt{P_{out}(\omega_0) * 2R_L} = \sqrt{20E-3*2*50} \approx 1.414V \quad \text{(C-1)}$$

The fundamental current is

$$I_{out}(\omega_0) = \frac{V_{out}(\omega_0)}{50} = \frac{1.414}{50} = 28.3mA \quad \text{(C-2)}$$

The DC operating point is calculated based on the normalized drive level x = 20. The expression for the emitter dc current can be given in terms of the Bessel function with respect to the drive level is

$$[I_E(\omega_0)] = 2I_{DC}\left[\frac{I_1(x)}{I_0(x)}\right]_{x=Normalized-Drive-Level} \quad \text{(C-3)}$$

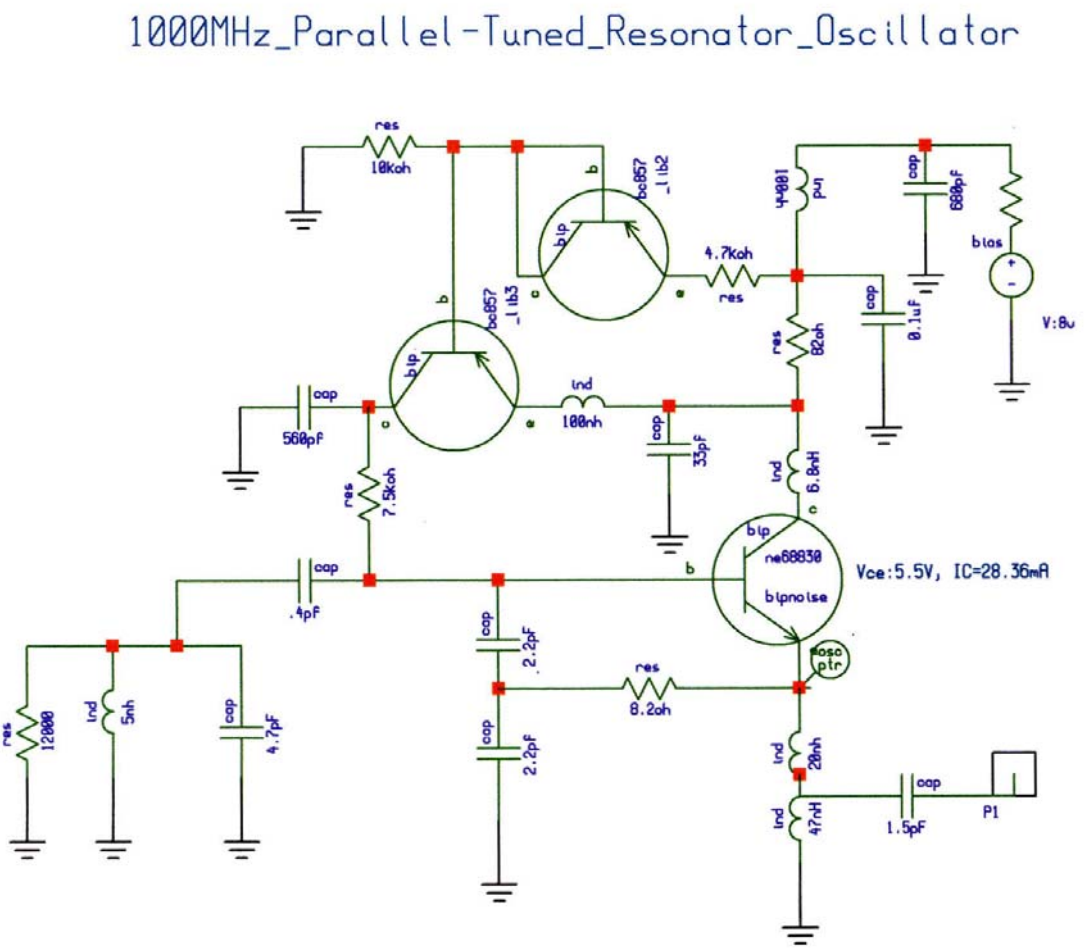


Figure C-1 Schematic of the 1000 MHz oscillator.

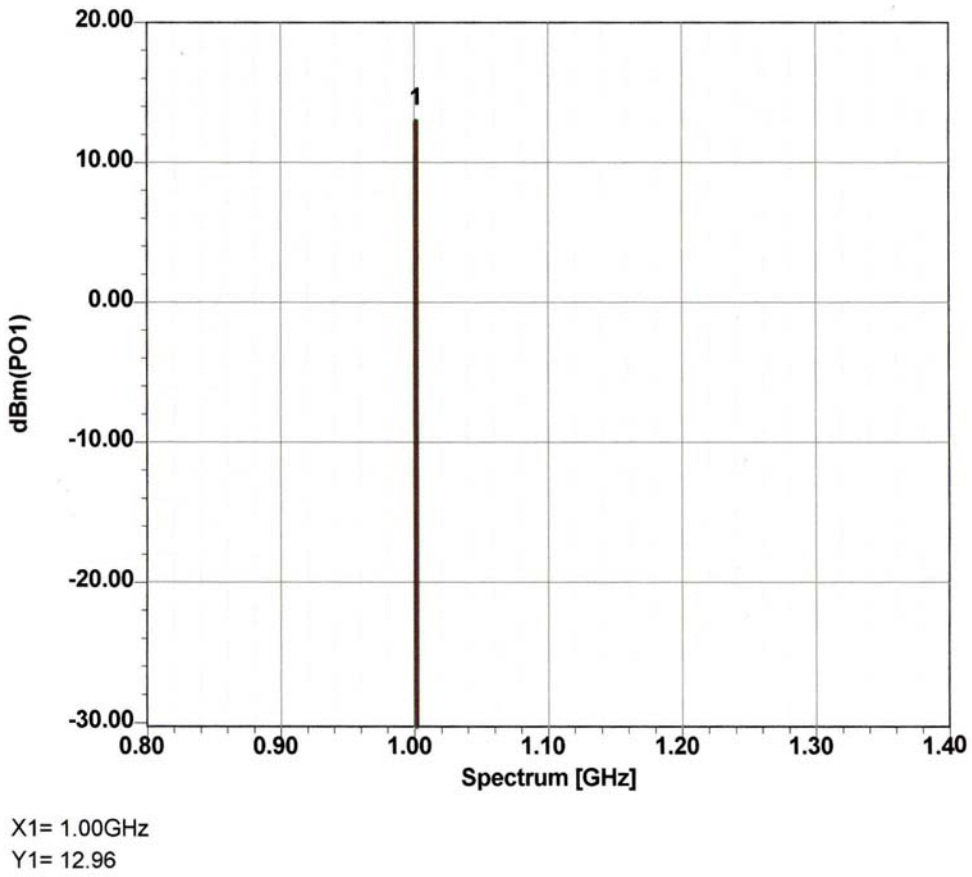


Figure C-2 Predicted output power of the oscillator.

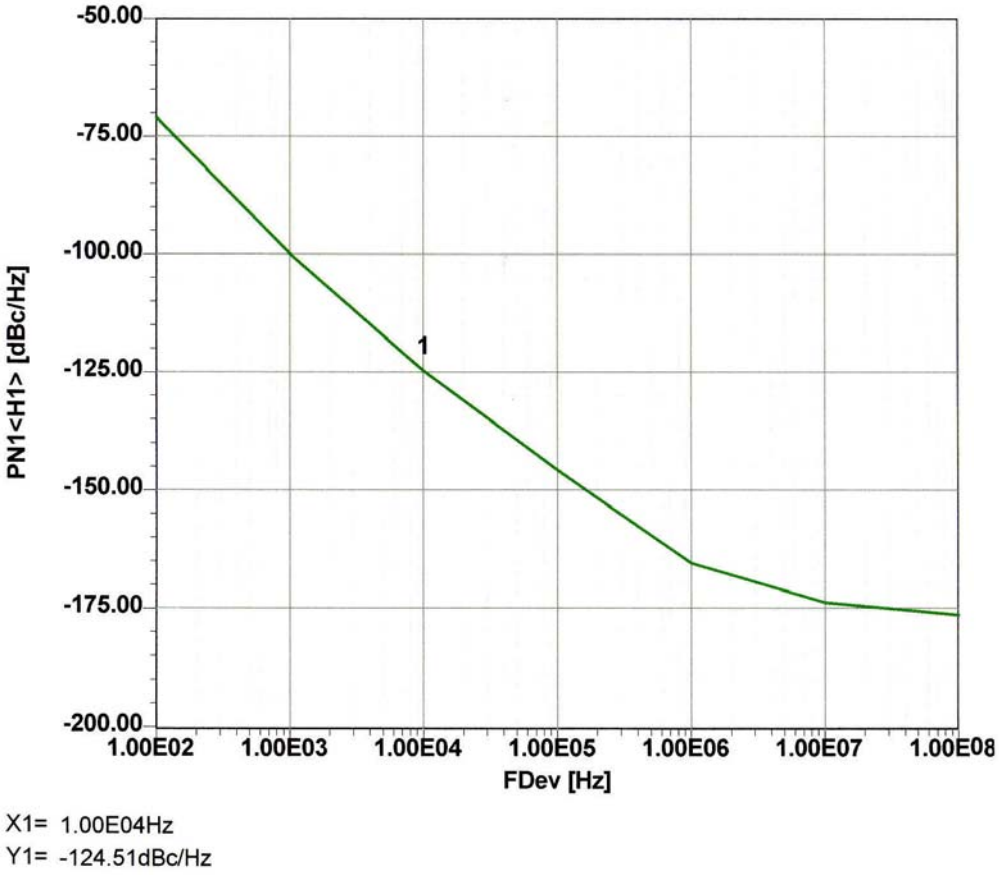


Figure C-3 Predicted phase noise of the oscillator.

For the normalized drive level x = 20, the output emitter current at the fundamental frequency can be given as

$$\left[I_E(\omega_0)\right]_{x=20} = \left[I_{E1}(\omega_0)\right]_{x=20} + \left[I_{E2}(\omega_0)\right]_{x=20} = 2I_{DC}\left[\frac{I_1(x)}{I_0(x)}\right]_{x=20} \approx 56mA \qquad \text{(C-4)}$$

$$\left[I_{E1}(\omega_0)\right]_{x=20} = I_{out}(\omega_0) = 28.3mA \text{ (output current to the load)} \qquad \text{(C-5)}$$

Figure C-4 shows the oscillator circuit configuration in which DC and RF current distribution is shown and divided into its components.

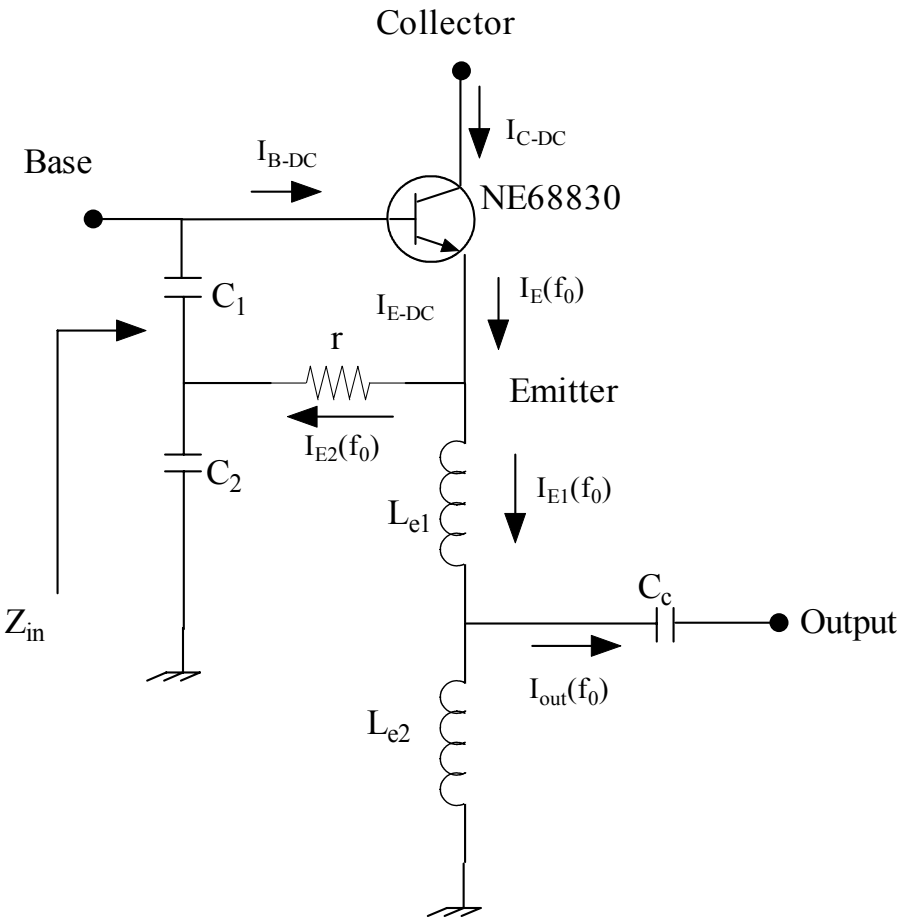


Figure C-4 Current distribution in the oscillator circuit.

$$\left[I_{E2}(\omega_0)\right]_{x=20} = \left[I_E(\omega_0)\right]_{x=20} - \left[I_{E1}(\omega_0)\right]_{x=20} = 27.3mA \tag{C-6}$$

$$I_{E-DC} = \frac{\left[I_E(\omega_0)\right]_{x=20}}{2\left[\frac{I_1(x)}{I_0(x)}\right]_{x=20}} = 28.3mA \tag{C-7}$$

For this application, the NE68830 was selected.

Step 2:

Biasing circuit

For the best phase noise close-in, a DC/AC feedback circuit is incorporated, which provides the desired operating DC condition [84]:

I_E=28.3mA

V_{CE}=5.5V, Supply Voltage V_{cc}=8V

β=120

I_B≈0.23mA

Step 3:

Calculation of the large-signal transconductance.

$$Y_{21}\Big|_{large-signal} = G_m(x) = \frac{qI_{dc}}{kTx}\left[\frac{2I_1(x)}{I_0(x)}\right]_{fundamental} \tag{C-8}$$

$$\left[Y_{21}\right]_{\omega=\omega_0} = \left[\frac{1.949 I_{E-DC}}{520mV}\right] = 0.107 \tag{C-9}$$

Step 4:

Loop Gain.

The loop gain is

$$Loop-Gain = [LG]_{sustained-condition} = \left[\frac{R_P Y_{21}(x)}{n}\right] = \left[\frac{R_P g_m}{x}\right]\left[\frac{2I_1(x)}{I_0(x)}\right]\left[\frac{1}{n}\right] > 1 \tag{C-10}$$

$$R_{PEQ}(f_0) = R_P \parallel Bias-circuit \Rightarrow 50.73\Omega \tag{C-11}$$

As earlier derived, the loop gain should be 2.1 to have good starting conditions!

$$n = \left[\frac{R_{PEQ} Y_{21}(x)}{2.1}\right] = \frac{0.107 * 50.73}{2.1} \approx 2.523 \tag{C-12}$$

Step 5:

Calculation of the feedback capacitor ratio.

$$n = 1 + \left[\frac{C_1}{C_2}\right] = 2.523 \Rightarrow \left[\frac{C_1}{C_2}\right]_{x=20} = 1.523 \ (2.523 - 1) \tag{C-13}$$

Step 6:

Calculation of absolute values of feedback capacitor.

The expression of Z_{in} (Looking in to the base of the transistor) can be given as

$$Z_{in} \cong -\left[\left(\frac{Y_{21}}{\omega^2 (C_1^* + C_p) C_2}\right)\left(\frac{1}{(1+\omega^2 Y_{21}^2 L_p^2)}\right)\right] - j\left[\left(\frac{(C_1^* + C_P + C_2)}{\omega (C_1^* + C_P) C_2}\right) - \left(\frac{\omega Y_{21} L_P}{(1+\omega^2 Y_{21}^2 L_p^2)}\right)\left(\frac{Y_{21}}{\omega (C_1^* + C_P) C_2}\right)\right] \tag{C-14}$$

where

$C_P = (C_{BEPKG}$ + contribution from layout) = 1.1pF

$L_P = (L_B + L_{BX}$ + contribution from layout) = 2.2nH.

The expression for the negative resistance R_n is

$$R_{neq} = \frac{R_n}{(1+\omega^2 Y_{21}^2 L_P^2)} = \frac{R_n}{[1 + (2\pi * 1E9)^2 * (0.107)^2 * (2.2nH)^2]} \tag{C-15}$$

$$R_{neq} \approx \frac{R_n}{3.65} \tag{C-16}$$

$$R_n = -\left[\frac{Y_{21}^{+}}{\omega^2 C_1 C_2}\right]_{x=20} = \frac{0.107}{(2\pi * 1E9)^2 C_1 C_2} \tag{C-17}$$

R_n is the negative resistance without parasitics (C_P, L_P).

For sustained oscillation $\rightarrow R_{neq} \geq 2\mathrm{R_{PEQ}} \cong 101.4$ Ohm

$$R_n = 3.65 * 101.4 \approx 371 Ohm \tag{C-18}$$

$$C_1 C_2 = \left[\frac{1}{\omega^2}\right]\left[\frac{0.107}{371}\right] \approx 7.26 \tag{C-19}$$

$$\left[\frac{C_1}{C_2}\right]_{x=20} \approx 1.52 \tag{C-20}$$

$$C_1 = 3.3 pF \tag{C-21}$$

$$C_2 = 2.2 pF \tag{C-22}$$

Step 7:

Calculation of the coupling capacitor r_e.

The expression for the coupling capacitor is

$$\frac{C}{10} > C_C > \left\{\frac{(\omega^2 C_1 C_2)(1+\omega^2 Y_{21}^2 L_P^2)}{[Y_{21}^2 C_2 - \omega^2 C_1 C_2)(1+\omega^2 Y_{21}^2 L_P^2)(C_1 + C_P + C_2)]}\right\} \tag{C-23}$$

$$C_c \rightarrow 0.4 pF \tag{C-24}$$

Figure C-5 shows the transistor in the package parameters for the calculation of the oscillator frequency and loop gain.

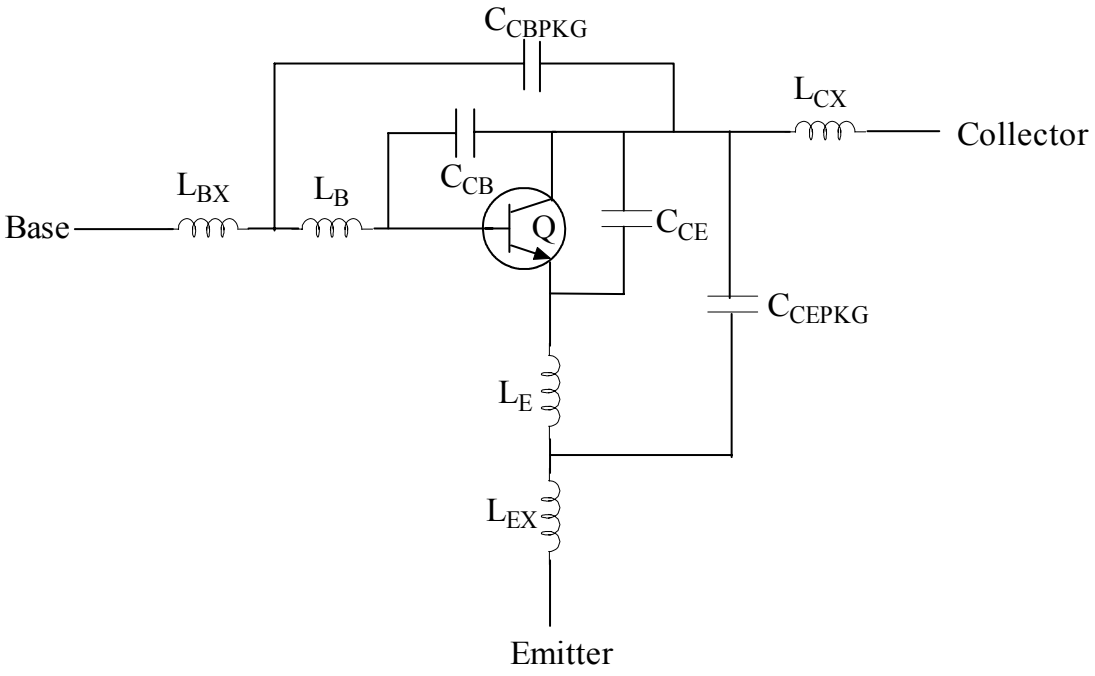


Figure C-5 NE68830 with package parasitics. Q is the intrinsic bipolar transistor.

Tables C-1 and C-2 show NE68830 nonlinear parameters and package parameters which were taken from the NEC data sheets.

Table C-1 Nonlinear parameters

Parameters	Q	Parameters	Q
IS	3.8E-16	MJC	0.48
BF	135.7	XCJC	0.56
NF	1	CJS	0
VAF	28	VJS	0.75
IKF	0.6	MJS	0
NE	1.49	TF	11E-12
BR	12.3	XTF	0.36
NR	1.1	VTF	0.65
VAR	3.5	ITF	0.61
IKR	0.06	PTF	50
ISC	3.5E-16	TR	32E-12
NC	1.62	EG	1.11
RE	0.4	XTB	0
RB	6.14	XTI	3
RBM	3.5	KF	0
IRB	0.001	AF	1
RC	4.2	VJE	0.71
CJE	0.79E-12	MJE	0.38
CJC	0.549E-12	VJC	0.65

Table C-2 Package parameters of NE68830

Parameters	NE68830
C_{CB}	0.24E-12
C_{CE}	0.27E-12
L_B	0.5E-9
L_E	0.86E-9
C_{CBPKG}	0.08E-12
C_{CEPKG}	0.04E-12
C_{BEPKG}	0.04E-12
L_{BX}	0.2E-9
L_{CX}	0.1E-9
L_{EX}	0.2E-9

Design Calculations

1. Frequency of Oscillation

Frequency of the oscillation is

$$\omega_0 = \sqrt{\frac{1}{L\left[\frac{\left[\frac{(C_1^* + C_P)C_2C_c}{(C_1^* + C_P + C_2)}\right]}{\left[\frac{(C_1^* + C_P)C_2}{(C_1^* + C_P + C_2)} + C_c\right]} + C\right]}} \approx 1000MHz \qquad \text{(C-25)}$$

with

L = 5nH (Inductance of the parallel resonator circuit)

$C_1^* = 2.2pF$

$C_1 = C_1^* + C_P$

C_P=1.1Pf (C_{BEPKG} + Contribution from layout)

$C_2 = 2.2pF$

$C_c = 0.4pF$

C =4.7pF

R_P=12000 (Measured)

$$Q_{unloaded} = \left[\frac{R_P}{\omega L}\right] = 380$$

2. Calculation of the Phase Noise

The noise equation which was determined in Chapter 8.4, Equations (8-109), (8-115), and (8-117), and which contains resonator noise, shot noise, and flicker noise, can now be used to graphically determine the best phase noise as a function of *n*. Figure C-6 shows a plot of this curve. It gives the best number of *n* to be 2.5, which is consistent with the calculation done for the large-signal condition. Eq. (C-12) gives the same result.

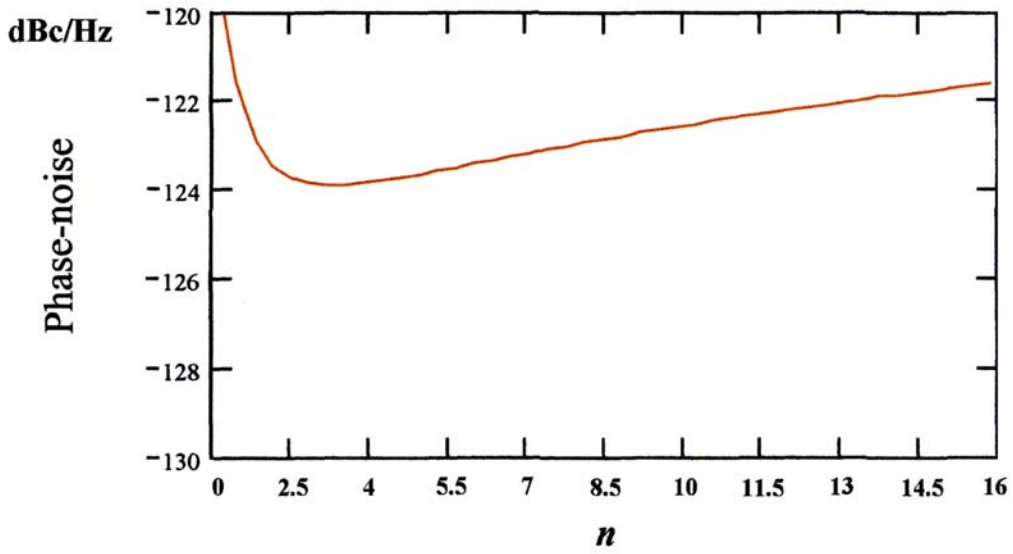


Figure C-6 The phase noise contribution of the lossy resonator at 10KHz offset.

The calculated phase noise at 10 KHz off the carrier is –124 dBc/Hz, which agrees with the measurements within 1 dB. The other values are –140 dBc/Hz at 100 kHz offset and –160 dBc/Hz at 1 MHz offset.

This circuit is shown in Chapter 9.1, Figure 9-2. The actual measured phase noise is shown in Figure 9-4, and the simulation is shown in Figure 9-5. Considering that Equation (8-109) only contains shot and flicker noise, as well as resonator noise, it has been proven that this by itself is a very accurate formula for practical use. Figure 9-5 has been generated from using Ansoft Designer, which includes all noise sources and is based on the harmonic balance principle.

The important conclusion found in Chapter 8 is that for the first time we have a complete mathematical synthesis procedure for best phase noise that covers both flicker noise and white noise for the oscillator. In the past, most publications have referenced an oscillator built with many shortcuts and then the author found that the measured results agree with the expectations. A complete synthesis approach has not appeared previously.

Oscillator Design Using LTSpice

By David Stockton, GM4ZNX

Modern RF design is heavily reliant on simulation. Universities have shifted emphasis from hardware labs to computer simulations. Simulators work well on amplifiers, filters, modulators, mixers and so on, but not as well on oscillators. This leaves even graduate-level RF engineers rather light on the subject of oscillators.

Such a void is a back-door opportunity to oscillator analysis. Simulation has not been used much by amateurs because it is computationally intensive. Most recent PCs have plenty of power for this task, however. You may not be aware of how powerful your machine is, because things like operating systems and word processor software have become progressively inefficient. Set your computer loose on a math-intensive task like circuit simulation and see what a beast has been hiding behind the flashy graphics and zillions of type fonts.

The simulator needs to be able to handle oscillators, and it needs to be affordable on an amateur budget. High-end RF CAD packages usually contain tools for handling oscillators, but they aren't easy to use and many are afterthought additions that don't mesh with the rest of the package. Oscillators are diabolical things to simulate. Even if you can afford to shovel money at the problem, it still takes a bit of creativity to use a full "bells and whistles" simulator on an oscillator and for the results to make sense. (For detailed information on simulation, see the chapter on **Computer-Aided Circuit Design**.)

An oscillator is a simple loop with signal flowing round and round in it. We can view the signal flow as being many components adding together at some point at some time. We can think of these components as being different vintages. This component came from thermal noise X microseconds ago and has been round the loop Y times, and that component… you can see the pattern. This is hard to analyze because all components get summed, not separated. So instead of thinking of our oscillator as a single stage with everything distributed in time, let's distribute it in space as well.

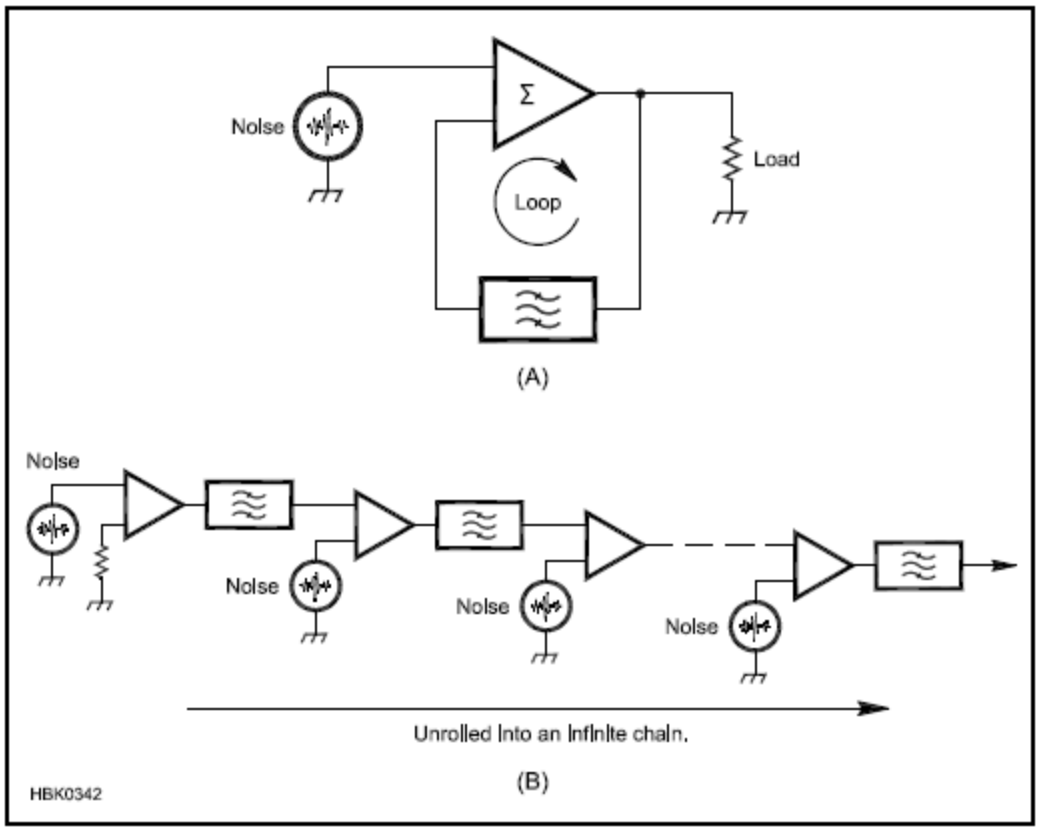


Figure 1 — The "Swiss Roll" visualization used by GM4ZNX. The amplifier loop is "unrolled" to permit its signals to be observed.

The GM4ZNX "Swiss-Roll" technique is to think of a rolled-up jelly cake and unroll the oscillator circuit as illustrated in **Figure 1**. We break the loop open, which leaves us with a tuned amplifier circuit with an input and an output terminal. In a closed oscillator loop, the output terminal would drive the input terminal. In the unrolled circuit, the output terminal drives the input of a second stage and so on.

Instead of infinitely looping signals in a single stage, we now have a single signal flow down an infinite string of stages. This doesn't sound any better, but we only need to handle a couple of hundred stages. Think about that… we are going to simulate a 200-stage tuned amplifier! But all the stages are identical, so we only have to draw one stage and have the others built as hierarchical repeats. On a 2005 model laptop, a simulation takes several minutes, which is fine.

Affordable RF analysis programs are normally limited to linear simulations and can't handle the oscillator's amplitude control mechanism. We also need a simulator that can handle random noise at the same time so the choice of tools becomes very limited. One example of a suitable

simulation package, based on *SPICE*, is available free from the Linear Technologies website, **www.linear.com**. (The program is called *SWCADIII* or *LTSpice*.) It is optimized for the analysis of switch-mode power supply (SMPS) circuits. This is very good for our purposes. In an SMPS things ring at high frequencies, and slow things settle. *LTSpice* has some trickery which allows it to easily handle RF speed events, while running a simulation efficiently over a long enough period for control loops to settle. This is what makes it efficient for oscillators. Our oscillator circuits are run at such large signal levels that as the oscillator reaches its long term output, it will affect bias conditions, which are slow-damped by decoupling components. (Again, refer to the **Computer-Aided Circuit Design** chapter for more information on circuit simulation.)

LTSpice can handle noise, and it can also handle hierarchical schematics. We draw our basic oscillator circuit once, and create a symbol for it. We can then use that symbol in a higher level schematic. For our worked example of an oscillator analysis, a single-stage schematic and symbol were created, then a higher level, a 10-pack of those symbols was created. The top level was made of 20 10-packs. Files for these designs are in the *Handbook's* companion CD, but to be able to set them up in *LTSpice* you will need to read *LTSpice's* help files on hierarchical designs. Hierarchical schematics save the need to draw our oscillator stage 200 times. It also allows editing a parameter on one schematic to change all 200 stages at once. Without this feature, things would be tedious.

Figure 2 shows a basic oscillator circuit. The transistor is a bipolar type, operated in common-base mode. The resonator is an LC tank with a capacitive tap. The common-base amplifier gives less than unity current gain, low input impedance and high output impedance. There has to be an impedance transformation to make the loop have enough gain to oscillate, and the capacitive tap is it. Instead of having bias resistor networks, the stage has a voltage source to set the collector bias voltage, and a current source to set the quiescent emitter current. You can just type in your bias values without having to calculate resistor values. One drawback of *LTSpice* is that it has few RF parts in its libraries, but a search on the Internet will find user groups and guidance on editing models for other *SPICE* variants to work with *LTSpice*. The 2N4142 in the supplied library is used in this example. A 5 V collector bias and 0.2 mA emitter bias have been chosen as starting points.

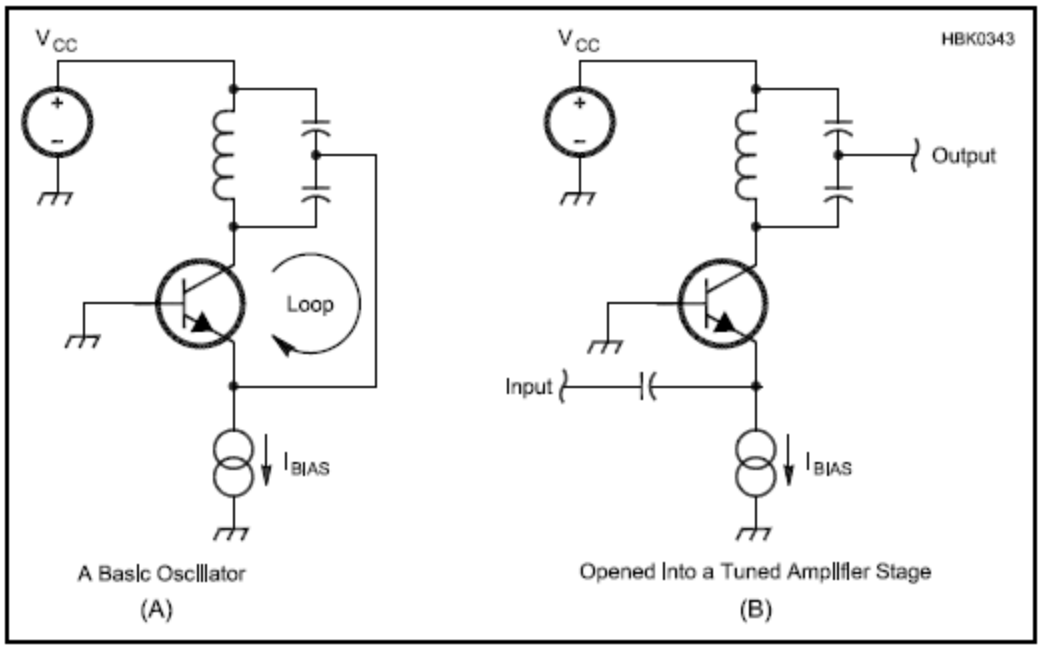


Figure 2 — The basic oscillator circuit (A) is built on a tuned amplifier circuit (B).

In designing this circuit, we must create a stage gain greater than unity, and allow the operating level to rise until that gain is compressed to exactly unity. With a bipolar transistor at RF, we do not want it to go into saturation. Instead, we want it to go into cut-off before that can happen. Set the emitter current for the level you want, and then make sure there is enough collector bias voltage that the instantaneous collector voltage is always a few volts more positive than the emitter. The L/C ratio of the tank, and the capacitive tap ratio are surprisingly tolerant, the circuit will oscillate with these parameters varied over an appreciable range. If your goal is low drift, then you should go for high capacitance in the tank, to dilute the effect of strays. If your goal is low phase noise, then you should try to create as high a tank Q as possible.

Because oscillators of this type use nonlinear device operation to control amplitude, do not try to get low levels of harmonics on their output — the harmonic creation mechanism is fundamental to the oscillator. Try an oscillator with a detector and feedback loop to control its level instead. The square-law characteristic of JFETs is an excellent level-stabilizing mechanism and accounts for their popularity in oscillators. However, their wide range of I_{DSS} for any given type, can be troublesome. MMIC amplifiers with internal feedback are probably the worst choice of device, but some types can be used in special circumstances.

In the simulation circuit provided here you will find some odd things. The random number source is of uniform density, so several of them are added together to approximate Gaussian noise. The collector load resistor which represents the output of the oscillator is split into two parts, a resistor to ground on the output is needed to define the dc potential of a node between the capacitors of adjacent stages (or else *SPICE* complains) and it also loads the tank via the tap.

When you have got all the schematics in the right directories for *LTSpice* to use them, and run the simulation, you will have an immense database of all waveforms at all nodes. You can now probe around the top level schematic. The first transistor in the chain acts as an emitter-follower so you can see its noise voltage coming out of its input if you probe there. The way the random number generators work is tied to the simulation time clock and you will see the first random number generator turn on at about 2 μs into the simulation, followed progressively by the others. This is just an oddity of the realization, but it does illustrate the summation of differently-seeded generators to approximate Gaussian distribution of noise.

Probing along, 10 stages at a time, you will see bigger and bigger noise waveforms until you start to notice the effect of the cumulative selectivity, as it starts to look like a noisy sine wave. Further along you will see the level begin to stabilize. If you zoom out to a larger time-scale, you will see that the sine wave seems to have low frequency random noise AM applied to it. As you probe further along you will see this "AM" compressed until it isn't seen, by the level control action of the oscillator and progressively narrowing bandwidth. Long before you get to the end of the 200 stages, you will have the appearance of a stable sine wave. Remember that the taps earlier in the structure represent the signal in a closed loop oscillator at times close to when it started-up. In a running oscillator, compression eventually reduces the gain of all amplification passes of all signal components. Fourier transform conversion can be used to convert these time-pictures into spectrum displays, if you want to explore further.

Among the accompanying files there is also a simulator that takes a single stage and plots its compression characteristic. It could be improved by adding earlier and later stages to make the source and load impedances more representative. The example oscillator can also have a model of a quartz crystal added in series with its output, to simulate a crystal oscillator. Explore! And have fun.

How can a lower phase noise oscillator be designed? Firstly if you use a lower noise transistor, it will take more stages of gain and filtering to bring it up to the stable output level.

The greater repetition of filtering before noise reaches a significant level narrows the bandwidth of the output signal. Secondly, if you can engineer a higher-Q tank circuit, each pass through the tank has a greater narrowing effect.

The simulation files for this section are included with this article:

SwissRollDemoBasicStage.asc — (The oscillator stage. Editing this changes every stage)

SwissRollDemoBasicStage.asy — (The symbol file for use in higher level schematics)

SwissRollDemo10Pack.asc — (10 basic stages as a building block)

SwissRollDemo10Pack.ass — (The symbol for a 10 pack)

SwissRollDemoTopLevel.asc — (This is the real simulation, uses the above as components)

SwissRollDemoCompression.asc — (Crude simulation showing stage gain compression)

SwissRollDemoStageBandwidth.asc — (Crude simulation showing filter Q of one stage)

7.3 Nonlinear Approach to the Calculation of Oscillator Phase Noise

By Dr. Ulrich L. Rohde, N1UL

The mechanism of noise generation in an oscillator combines the equivalent of frequency conversion (mixing) with the effect of AM-to-PM conversion. Therefore, to calculate oscillator phase noise, we must first be able to calculate the noise figure of a mixer [75]. This chapter presents the use of an algorithm for the computation of SSB carrier noise in free running oscillators using the harmonic balance (HB) nonlinear technique.

Traditional approaches relying on frequency conversion analysis are not sufficient to describe the complex physical behavior of a noisy oscillator. The accuracy of this nonlinear approach is based on the dynamic range of the harmonic balance simulator and the quality of the parameter extraction for the active device. The algorithm described has also been verified with several examples up to millimeter wavelengths. This is the only algorithm that provides a complete and rigorous treatment of noise analysis for autonomous circuits without restrictions such as not being able to handle memory effects.

Noise Generation in Oscillators

As shown above, the qualitative linearized picture of noise generation in oscillators is very well known. The physical effects of random fluctuations taking place in the circuit are different depending on their spectral allocation with respect to the carrier:

- Noise components at low frequency deviations result in frequency modulation of the carrier through mean square frequency fluctuation proportional to the available noise power.
- Noise components at high frequency deviations result in phase modulation of the carrier through mean square phase fluctuation proportional to the available noise power.

We will demonstrate that the same conclusions can be quantitatively derived from the HB equations for an autonomous circuit.

Equivalent Representation of a Noisy Nonlinear Circuit

A general noisy nonlinear network can be described by the equivalent circuit shown in Figure 7-13 and Appendix D. The circuit is divided into linear and nonlinear subnetworks as noise-free mult8-ports. Noise generation is accounted for by connecting a set of noise voltage and noise current sources at the ports of the linear subnetwork [76-80].

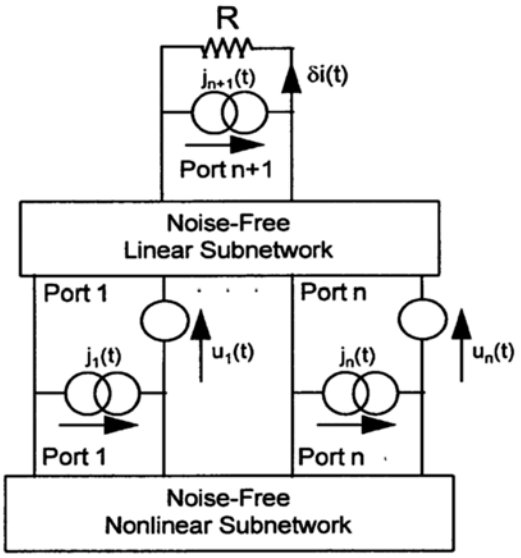


Figure 7-13 Equivalent circuit of a general noisy nonlinear network.

Frequency Conversion Approach

The circuit supports a large signal time periodic steady state of fundamental angular frequency ω_0 (carrier). Noise signals are small perturbations superimposed on the steady state, represented by families of pseudo-sinusoids located at the sidebands of the carrier harmonics. Therefore, the noise performance of the circuit is determined by the exchange of the power among the sidebands of the unperturbed steady state through frequency conversion in the nonlinear subnetwork. Due to the perturbative assumption, the nonlinear subnetwork can be replaced with a mult8-frequency linear mult8-port described by a conversion matrix. The flow of noise signals can be computed by means of conventional linear circuit techniques.

The frequency conversion approach frequently used has the following limitations:

The frequency conversion approach is not sufficient to predict the noise performance of an autonomous circuit. The spectral density of the output noise power, and consequently the PM noise computed by the conversion analysis are proportional to the available power of the noise sources.

- In the presence of both thermal and flicker noise sources, PM noise: raises as ω^{-1} for $\omega \to 0$; tends to a finite limit for $\omega \to \infty$.

- Frequency conversion analysis: correctly predicts the far carrier noise behavior of an oscillator, and in particular the oscillator noise floor; does not provide results consistent with the physical observations at low deviations from the carrier.

This inconsistency can be removed by adding the modulation noise analysis. In order to determine the far away noise using the autonomous circuit perturbation analysis, the following applies:

The circuit supports a large signal time periodic autonomous regime. The circuit is perturbed by a set of small sources located at the carrier harmonics and at the sidebands at a deviation ω from carrier harmonics. The perturbation of the circuit state $(\delta \mathbf{X}_B, \delta \mathbf{X}_H)$ is given by the uncoupled sets of equations:

$$\frac{\partial E_B}{\partial E_B} \delta X_B = J_B(\omega) \tag{7-36}$$

$$\frac{\partial E_H}{\partial E_H} \delta X_H = J_H(\omega) \tag{7-37}$$

where

E_B, E_H = vectors of HB errors
X_B, X_H = vectors of state variable (SV) harmonics (since the circuit is autonomous, one of the entries X is replaced by the fundamental frequency ω_0)
J_B, J_H = vectors of forcing terms

The subscripts B and H denote sidebands and carrier harmonics, respectively.

For a spot noise analysis at a frequency ω, the noise sources can be interpreted in either of two ways:

- Pseudo-sinusoids with random amplitude and phase located at the sidebands. Noise generation is described by Equation (7-36) which is essentially a frequency conversion equation relating the sideband harmonics of the state variables and of the noise sources. This description is exactly equivalent to the one provided by the frequency conversion approach. This mechanism is referred to as *conversion noise* [70-79].

- Sinusoids located at the carrier harmonics, randomly phase- and amplitude-modulated by pseudo-sinusoidal noise at frequency ω. Noise generation is described by Equation (7-37), which describes noise-induced jitter of the circuit-state, represented by the vector δX_H. The modulated perturbing signals are represented by replacing the entries of J_H with the complex modulation laws. This mechanism is referred to as *modulation noise*. One of the entries of δX_H is $\delta\omega_0$

where $\delta\omega_0(\omega)$ = phasor of the pseudo-sinusoidal components of the fundamental frequency fluctuations in a 1 Hz band at frequency ω. Equation (7-37) provides a frequency jitter with a mean square value proportional to the available noise power. In the presence of both thermal and flicker noise, PM noise raises as ω^{-3} for $\omega \to 0$ and tends to 0 for $\omega \to \infty$. Modulation noise analysis correctly describes the noise behavior of an oscillator at low deviations from the carrier and does not provide results consistent with physical observations at high deviations from the carrier.

The combination of both phenomenon explains the noise in the oscillator shown in Figure 7-14, where the near carrier noise dominates below ω_X and far carrier noise dominates above ω_X. Figure 7-15 (itemized form) shows the noise sources as they are applied at the IF. We have arbitrarily defined the low oscillator output as IF. This applies to the conversion matrix calculation.

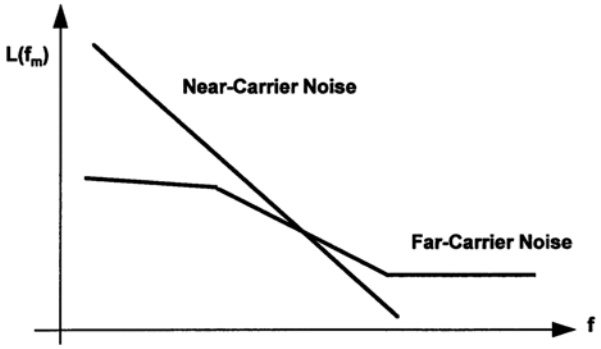


Figure 7-14 Oscillator noise components.

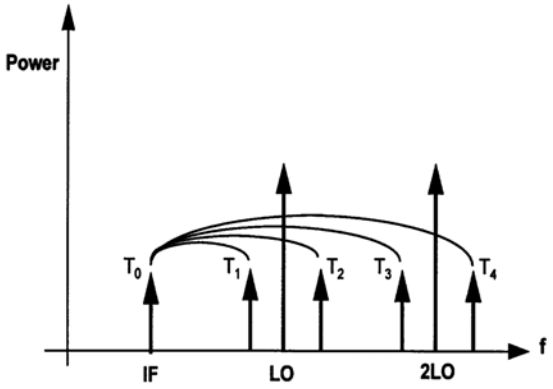


Figure 7-15 Noise sources where the noise at each sideband contributes to the output noise at the IF through frequency conversion.

Figure 7-16 shows the total contribution which have to be taken into consideration for calculation of the noise at the output. The accuracy of the calculation of the phase noise depends highly on the quality of the parameter extraction for the nonlinear device; in particular, high frequency phenomena must be properly modeled. In addition, the flicker noise contribution is essential. This is also valid for mixer noise analysis.

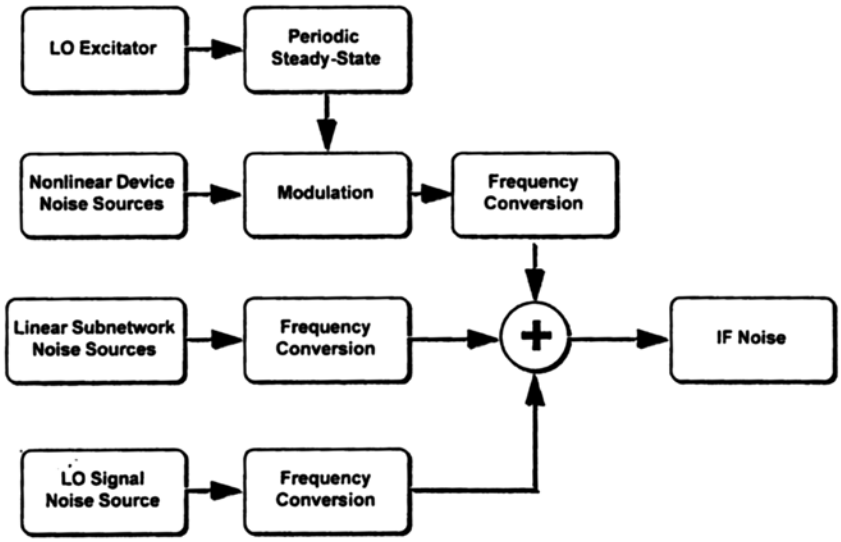


Figure 7-16 Noise mechanisms.

Conversion Noise Analysis

The actual mathematics used to calculate the noise result (Ansoft Serenade 8.*x*) are as follows:

*k*th harmonic PM noise:

$$\left\langle \left|\delta\Phi_k(\omega)\right|^2 \right\rangle = \frac{N_k(\omega) - N_{-k}(\omega) - 2\,\mathrm{Re}\left[C_k(\omega)\right]}{R\left|I_k^{SS}\right|^2} \tag{7-38}$$

*k*th harmonic AM noise:

$$\left\langle \left|\delta A_k(\omega)\right|^2 \right\rangle = 2\,\frac{N_k(\omega) - N_{-k}(\omega) + 2\,\mathrm{Re}\left[C_k(\omega)\right]}{R\left|I_k^{SS}\right|^2} \tag{7-39}$$

*k*th harmonic PM-AM correlation coefficient:

$$C_k^{PMAM}(\omega) = \left\langle \delta\Phi_k(\omega)\delta A_k(\omega)^* \right\rangle = -\sqrt{2}\,\frac{2\,\mathrm{Im}[C_k(\omega)] + j[N_k(\omega) - N_{-k}(\omega)]}{R\left|I_k^{SS}\right|^2} \tag{7-40}$$

where

$N_k(\omega)$, $N_{-k}(\omega)$ = noise power spectral densities at the upper and lower sidebands of the *k*th harmonic
$C_k(\omega)$ = normalized correlation coefficient of the upper and lower sidebands of the *k*th carrier harmonic
R = load resistance
I_k^{ss} = *k*th harmonic of the steady-state current through the load.

Modulation Noise Analysis

*k*th harmonic PM noise:

$$\left\langle \left|\delta\Phi_k(\omega)\right|^2 \right\rangle = \frac{k^2}{\omega^2}\mathbf{T}_F \left\langle \mathbf{J}_H(\omega)\mathbf{J}_H^t(\omega) \right\rangle \mathbf{T}_F^t \tag{7-41}$$

*k*th harmonic AM noise:

$$\left\langle \left|\delta A_k(\omega)\right|^2 \right\rangle = \frac{2}{\left|I_k^{SS}\right|^2}\mathbf{T}_{Ak} \left\langle \mathbf{J}_H(\omega)\mathbf{J}_H^t(\omega) \right\rangle \mathbf{T}_{Ak}^t \tag{7-42}$$

*k*th harmonic PM-AM correlation coefficient:

$$C_k^{PMAM}(\omega) = \left\langle \delta\Phi_k(\omega)\delta A_k(\omega)^* \right\rangle = \frac{k\sqrt{2}}{j\omega\left|I_k^{SS}\right|^2}\mathbf{T}_F \left\langle \mathbf{J}_H(\omega)\mathbf{J}_H^t(\omega) \right\rangle \mathbf{T}_{Ak}^t \tag{7-43}$$

where

$J_H(\omega)$ = vector of Norton equivalent of the noise sources
T_F = frequency transfer matrix
R = load resistance
I_k^{ss} = *k*th harmonic of the steady-state current through the load

Experimental Variations

We will look at two examples where we compare predicted and measured data. Figure 7-17 shows the abbreviated circuit of a 10 MHz crystal oscillator. It uses a high

precision, high Q crystal made by companies such as Bliley. Oscillators like this are intended for use as frequency and low phase noise standards. In this case, the circuit under consideration is part of the HP3048 phase noise measurement system.

Figure 7-18 shows the measured phase noise of this HP frequency standard, and Figure 7-19 shows the phase noise predicted using the mathematical approach outlined above.

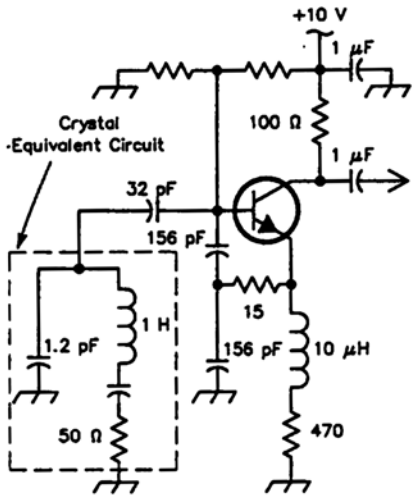


Figure 7-17 Abbreviated circuit of a 10-MHz crystal oscillator.

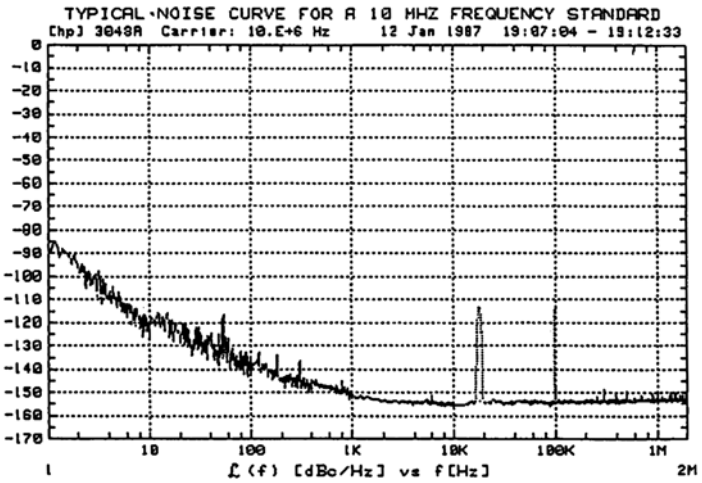


Figure 7-18 Measured phase noise for this frequency standard by HP.

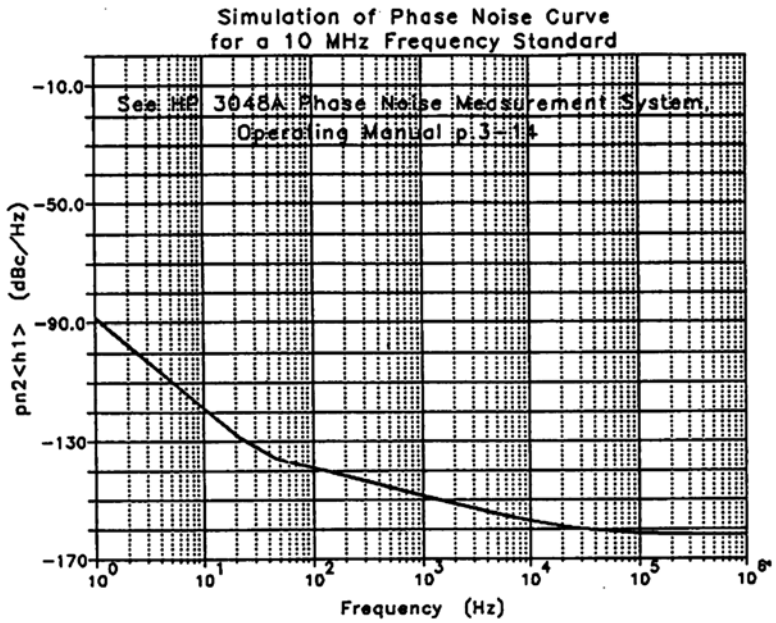


Figure 7-19 Simulated phase noise of the oscillator shown in Figure 7-17.

In co-operation with Motorola, an 800 MHz VCO was analyzed. The parameter extraction for the Motorola transistor was done. Figure 7-20 shows the circuit, which is a Colpitts oscillator that uses RF feedback in the form of a 15 Ω resistor between the emitter and the capacitive voltage divider. The tuned circuit is loosely coupled to this part of the transistor circuit. Figure 7-21 shows a plot of the measured and predicted phase of this circuit..

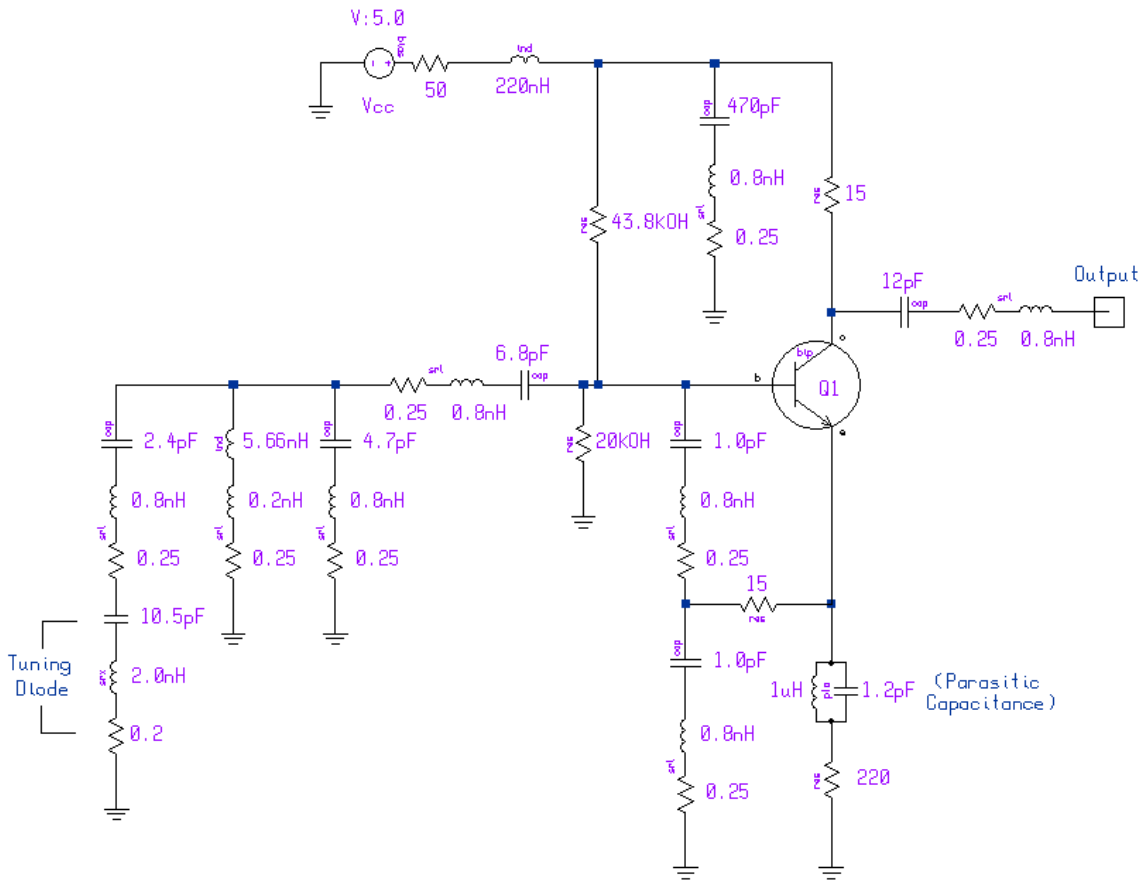


Figure 7-20 Colpitts oscillator that uses RF negative feedback between the emitter and capacitive voltage divider. To be realistic, we have also used real components rather than ideal ones. The suppliers for the capacitors and inductors provide some typical values for the parasitics. The major changes are 0.8 nH and 0.25 Ω in series with the capacitors. The same thing applies for the main inductance, which has a parasitic connection inductance of 0.2 nH in series with a 0.25 Ω resistance. These types of parasitics are valid for a fairly large range of components assembled in surface mount applications. Most engineers model the circuit only by assuming lossy devices, not adding these important parasitics. One of the side effects we have noticed is that the output power is more realistic and, needless to say, the simulated phase noise agrees quite well with measured data. This circuit can also serve as an example for modeling amplifiers and mixers using surface mount components.

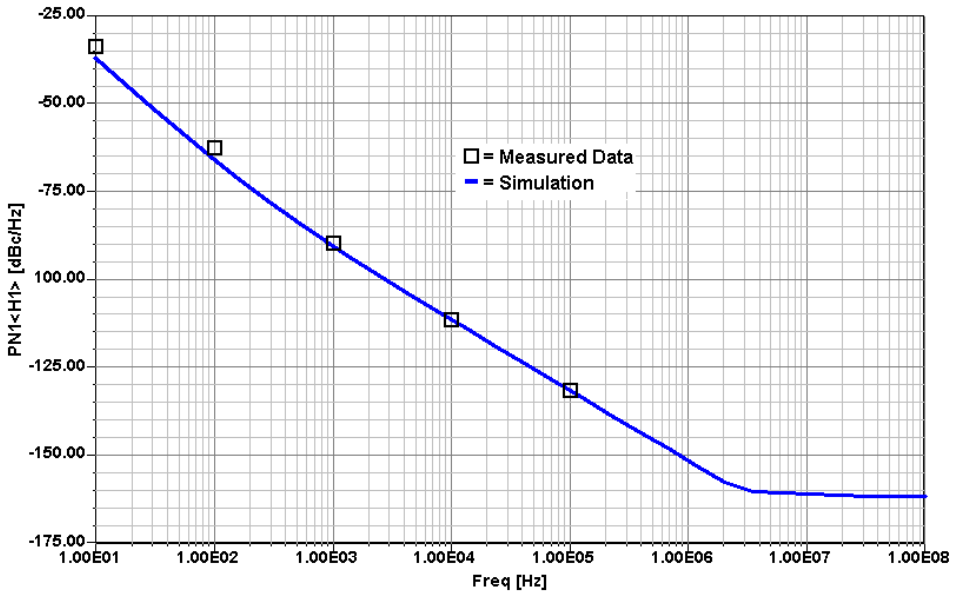


Figure 7-21 Comparison between predicted and measured phase noise for the oscillator shown in Figure 7-20.

The harmonic balance simulator Microwave Harmonica/Designer, which has been used for many cross-checks, is based on the principle shown above and shows extremely high accuracy in noise predictions. The harmonic balance simulator cannot be substituted by a set of equations because the harmonic balance process works iteratively, therefore, such a simulator is necessary in parallel to all the equations which are being derived to be used as a validation tool. An extreme example of its usefulness was the case where one of the previously shown oscillators was optimized for best output power with an assumed Q of 200 of the resonator circuit itself. In a following simulation, the value of Q was increased from 200 to 400 to examine the results. The output power remained the same, but the phase noise deteriorated. This contradicts practical experience for optimized oscillators. The surprising result can be explained by the fact that a particular parallel resonant value was assumed, and the values of C_1 and C_2 were calculated. By increasing the Q, the feedback ratio generated too much gain, more than necessary, and therefore, the phase noise became worse. This is an experiment which is normally not done when building oscillators, but shows the power of the CAD tool and the insight it provides into the inner workings of the oscillator.

Quartz Crystal Oscillator Design

Introduction :

In many applications, electromechanical resonators, such as quartz crystals are used as frequency selective element. Quartz crystals have the property of piezoelectricity. Devices with piezoelectric effect undergo mechanical deformation with the influence of applied electric charge and vice-a-versa. Due to this property, they are primarily used to form a resonator in oscillator circuit. Most of the communication systems rely on the quartz crystal as reference oscillator for synthesis of the harmonic signal required for their operation. The crystal (reference) oscillators are design for a stable reference frequency oscillator of 10MHz or 5Mhz and recently the higher frequency 100MHz or 120MHz for frequency synthesizers. Many of them are synchronized against Rubidium or Cesium standards.

The modern communication systems are particularly susceptible to reference oscillator phase noise because the process of frequency multiplication increases the power in the sidebands by the square of the multiplication factors. The phase noise of these sources limits the noise floor and interference susceptibility that affects directly the system performance, like bit error rate in point to point radios, range and load capability of telephone networks, reliability of navigation systems, detection ability of radars etc. Therefore designing low phase noise crystal oscillator is challenging for a given cost, size and power-consumption.

Any oscillator including such with extremely high Q transfers DC energy to RF energy, with some key parameter being most important.

These are: Extremely low phase noise
Short term and long term stability (aging)
Specified RF power output and low harmonic content
Pushing and pulling
DC power supply and DC tuning voltage to name a few

Here is a typical Data sheet from one of the world's best oscillator manufacturer

Wenzel Associates, Inc.
"Quietly the Best"

Crystal Oscillators > 4 to 30 MHz > HF Ultra Low Noise OCXO

Features:

- Lowest Phase Noise Available
- Good Frequency Stability over Temperature
- Internal Voltage Regulator
- Very Low Aging Rate

Applications:

- Radar Systems
- Reference for Phase Noise Measurements
- Synthesizers

Typical Specifications:						
Frequency *(Specify)*		4 to 30 MHz				
Frequency		5		10		MHz
Output Level		+13				dBm
Aging		$\pm 1 \times 10^{-9}$ to $\pm 1 \times 10^{-10}$ / day after 30 days				
Phase Noise						
	10 Hz	-115	-120	-130	-132	dBc/Hz
	100 Hz	-145	-150	-158	-162	dBc/Hz
	1 kHz	-165	-170	-172	-172	dBc/Hz
	10 kHz	-176	-176	-172	-175	dBc/Hz
Temperature Stability *(Specify)*		$\pm 5 \times 10^{-8}$ to $\pm 2 \times 10^{-8}$				
Range A	0 to +50C					
Range B	0 to +65C					
Range C	0 to +70C					
Range D	-20 to +70C					
Range E	-40 to +70C					
Range F	-55 to +85C					
Electrical Tuning Range *(Specify)*		$\pm 2 \times 10^{-7}$ to $\pm 2 \times 10^{-6}$				
Tuning A	0 to +10 VDC					
Tuning B	±5 VDC					
Supply Voltage *(Specify)*		+12 or +15				VDC
Warm-up Power		5 for 5 minutes				Watts
Total Power *typical*		2.5 @ 25°C				Watts
Crystal Type		SC				
Dimensions		44.4 x 74.7 x 25.4 1.75 x 2.94 x 1				mm inches
Connectors		SMA on side and solder pins on base				

These high performance oscillator are typically available in 5 MHz, 10 MHz, 80 MHz, 100 MHz and up to 120 MHz The higher frequency value oscillators are mostly voltage controlled crystal oscillators (VCXOs), but even the 5 MHz versions have a very small tuning range synchronize them with atomic frequency standards

Visiting Crystal Theory:

In many applications, electromechanical resonators, such as quartz crystals are used as frequency selective element. Quartz crystals have the property of piezoelectricity. Devices with piezoelectric effect undergo mechanical deformation with the influence of applied electric charge and vice-a-versa. Due to this property, they are primarily used to form a resonator in oscillator circuit. The commonly found resonators in the microwave/RF designs other than crystal resonators are LC, Microstrip, Ceramic, Dielectric, and YIG. Though each resonator has its advantage and disadvantage for use in particular application, generally the crystal oscillators are preferred as an option to design a stable reference frequency oscillator of 10MHz or 5Mhz and recently the higher frequency 100MHz or 120MHz for frequency synthesizers. These quartz crystal resonators suffer from multi-mode resonances and cross-talk due to large holding capacitance.

Figure (1) shows the typical impedance characteristics of electromechanical crystal resonator, which vibrates due to piezoelectric effect and exhibits multimode resonances.

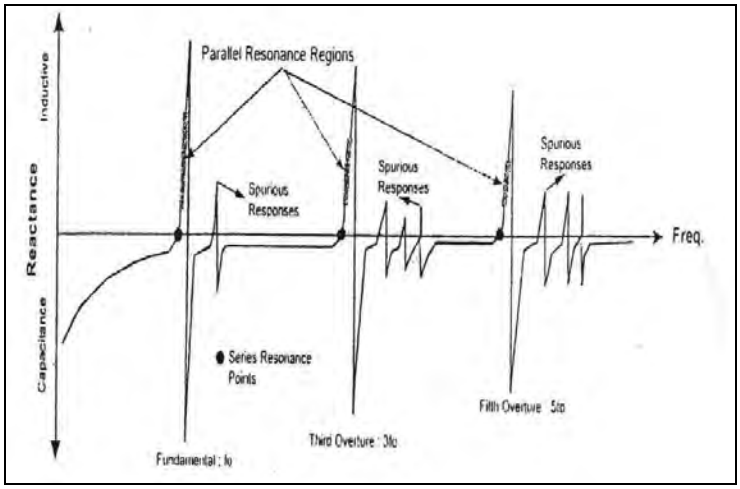


Figure 1: Fundamental and the overtone resonance [3]

Crystal Resonator: The crystal resonator is obtained from the abundant natural resource of quartz. The quartz stone gets cut into thin slices called “blank”, which are coated with metallic films that form the leads for exciting the crystal. The quartz is cut in various ways either in single rotation or double rotation, which results in significant change in the operating parameters mainly the operational frequency stability. This is more elaborated in the [1], [2] and [3] references. The commonly used blanks are formed from AT cut and SC cut quartz. The cut of the quartz also results in additional resonances, specifically in SC and IT cut crystals. These additional resonances termed as b-mode are located at approximately 10% higher in frequency from the desired c-mode. Apart from b-mode we also get the

a-mode resonance at a $\frac{188}{100}$ times the c-mode. The accompanying figure (2), explains position of modes for an SC cut crystal resonator.

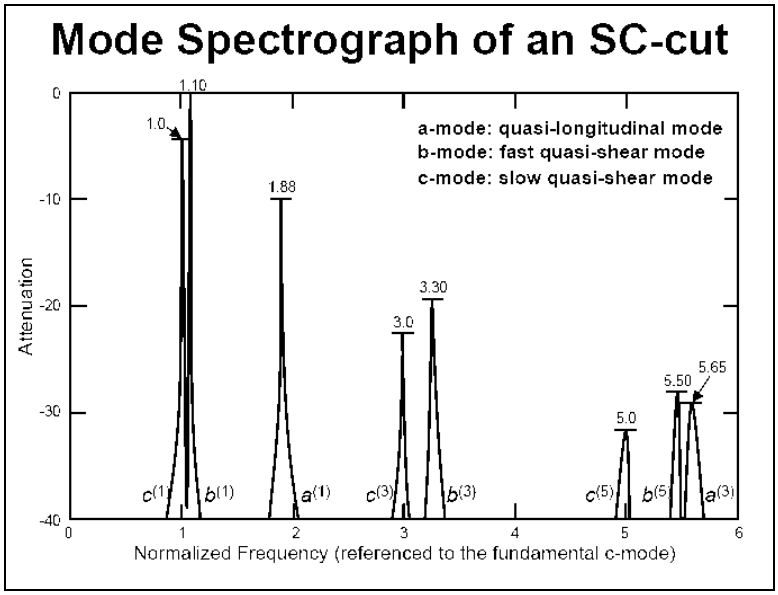


Figure 2: Modes for an SC cut Crystal resonator [2]

B-mode: The b-mode has a linear temperature characteristics and can be used as a sensitive thermometer of the resonator temperature. This effect has been used to design extremely stable microcomputer-compensated oscillators, where the frequency of b-mode ia used to compensate the fundamental mode and oscillations are present on both modes at all times.However more typically its required the crystal is operated only on a single mode. A resonant circuit must then be employed to trap out the b-mode and force the oscillations to occur on the desired mode at all times. This is b-mode trapping. Depending upon the circuit configuration, several different methods can be employed. This can be accomplished in Colpitts and Pierce oscillator by forcing one of the capcitive element to be inductive at the frequency of unwanted mode. As shown below the inductors L2 and C2 are series resonant at freuqency just below the b-mode. This means that they appear inductive at the b-mode frequency, thus they serve as b-mode trap. The net impedance of this circuit is shown below:

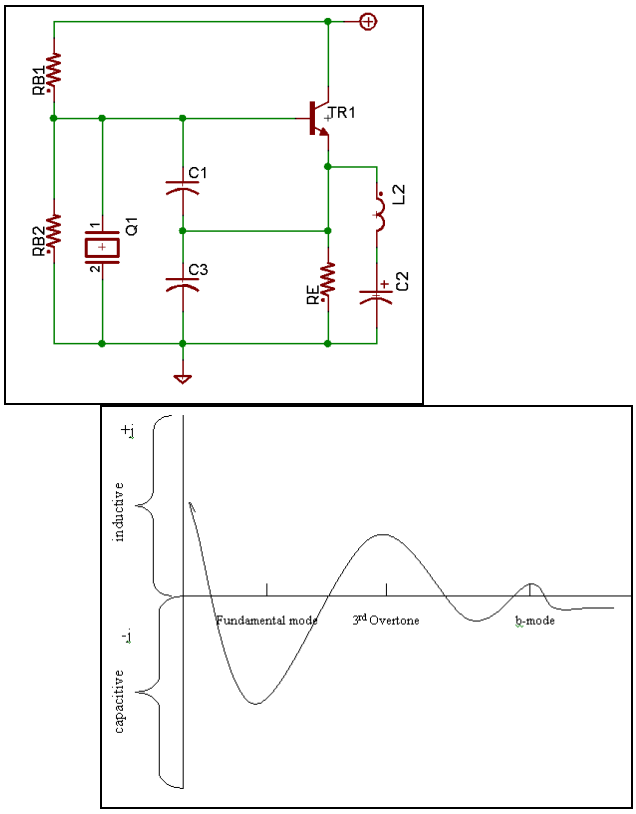


Figure 3: b-mode trap schematic and the net impedance for b-mode trap.

It can be very convenient to measure thermal performance of an oven using the b-mode. By returning the resonant circuit to force oscillations to occur on the b-mode, the linear frequency verses temperature characteristics can provide a means to precisely measureing the performance of the thermal enclosure. To accomplish this, the frequency variations caused by temperature changes of the b-mode are first measured with the oven off. This step provides a measn of characterizing the frequency-temperature characteristics of the b-mode. Next, the frequency change caused by external temperature variations are computed from this. Of course, the trap can then be retuned to set the oscillation back to the desired mode.

The equivalent circuit of a crystal at resonance can be shown as a series combination of RLC in parallel with a holding capacitor. The package capacitances and lead inductance are generally ignored till the VHF frequencies. The equivalent circuit for crystal shows two resonances, one due to the series branch alone and the other with the inductor L in combination with the effective capacitance of C0 and C1…Cn. These resonances are called the series resonant frequency and the anti-resonant frequency of the crystal and computed as,

$$fs = \frac{1}{2\pi\sqrt{L1\,C1}} \quad \text{and} \quad fp = \frac{1}{2\pi\sqrt{L1\left(\frac{C1\;C0}{C1+C0}\right)}}$$

where, *'fs'* is series resonant frequency and *'fp'* is the anti-resonant frequency [1].

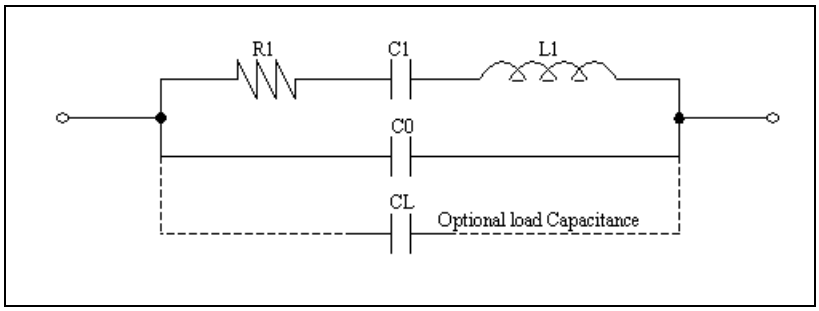


Figure 4: Equivalent Circuit of a crystal resonator with the optional CL capacitor [1]

When an oscillator presents some amount of load capacitance to a crystal, the crystal is said to be *parallel resonant*, and a value of load capacitance, CL, must be specified. If the circuit does not exhibit capacitive loading, the crystal is said to be *series-resonant*, and no value of load capacitance is specified. It is important to note that when a capacitor is placed in series with a crystal, the new series frequency is displaced slightly to a higher frequency than the original series resonance. Conversely, when the capacitor is placed in parallel with the resonator, the new parallel resonant frequency is displaced slightly to a lower frequency. This phenomenon has caused a great deal of perplexity between the terms series and parallel resonance. Series mode resonance of the crystal is represented by a small resistance in series with a resonant reactance, whereas, in parallel mode by a large resistor in parallel to a resonant susceptance. The series (f_i) and parallel resonance (f_p) are described by the impedance function,

$$Z(s) = \frac{1}{sC_0 + \dfrac{1}{1/sC_i + sL_i + R_i}} = \frac{s^2 + sR_i/L_i + 1/L_iC_i}{sC_0[s^2 + sR_i/L_i + (C_0 + C_i)/L_iC_iC_0]}$$

The further evaluation from the imaginary part of the zeroes

$$s_{z1,2} = -\frac{\omega_0}{2Q} \pm j\omega_0\sqrt{1 - \frac{1}{4Q^2}} \quad \approx \quad -\frac{\omega_0}{2Q} \pm j\omega_0, \quad for \quad Q >> 1$$

and poles as below,

$$s_{p1,2} = -\frac{\omega_0}{2Q} \pm j\omega_0\sqrt{1 + \frac{C_i}{C_0} - \frac{1}{4Q^2}} \approx -\frac{\omega_0}{2Q} \pm j\omega_0\left(1 + \frac{C_i}{2C_0}\right)$$

$$\omega_i = \frac{1}{\sqrt{L_iC_i}} \Rightarrow f_s(series) = \frac{1}{2\pi\sqrt{L_iC_i}}$$

$$\omega_p \approx \omega_0\left(1 + \frac{C_i}{2C_0}\right)\Big|_{C_0 >> C_i} \Rightarrow f_p(parallel) \approx \frac{1}{2\pi\sqrt{L_iC_i}}\left(1 + \frac{C_i}{2C_0}\right)\Big|_{C_0 > C_i}$$

$$M = \frac{2Q(\omega_p - \omega_0)}{\omega_0} = \frac{2Q(f_p - f_0)}{f_0}$$

gives us M, mode separation (f_p - f_0) equation. The degree to which an oscillator generates a constant frequency f_i throughout a specified period of time is defined as the frequency stability of the signal source.

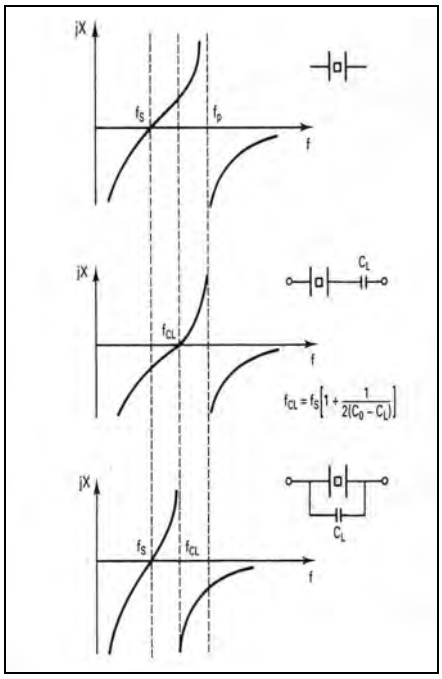


Figure 5: Crystal resonance with and with out the effects of load capacitance, *CL*.

Crystal does not produce harmonics and the overtone response of crystal is not harmonics of fundamental. For designing the high performance crystal oscillator, the oscillator circuit topology determines the crystal configuration, like use of fundamental, overtone, parallel and the series configuration. In other words, the oscillator circuit topology forces the crystal resonator into either the fundamental (lowest major resonant response), overtone (major responses other than fundamental), parallel (one of the inductive regions of the crystal's reactance curve) or series mode (one of the resistive points on the crystal's reactance curve) of operation.

For overtones the equivalent circuit of crystal gets an additional branch in parallel with a combination of RLC (not shown in above diagram). The values of R, L and C in the overtone branch can be computed by scaling the values of R, L and C in the fundamental resonant branch. If '*f*1' is the fundamental frequency then the nth overtone frequency should be computed as,

$$fn = n * f1 = \frac{1}{2\pi\sqrt{Ln\ Cn}} = \frac{n}{2\pi\sqrt{L1\ C1}} = \frac{1}{2\pi\sqrt{L1\frac{C1}{n^2}}}$$

$$\Rightarrow Ln = L1$$

$$\Rightarrow Cn = \frac{C1}{n^2} \quad where, n\ is\ 3,5,7\ etc\ldots\ overtone\ number$$

Wide pull Voltage controlled crystal oscillator (VCXO) typically utilizes fundamental crystals with large motional capacitance C1. Overtone operation is

precluded if wide tuning range is desired. Also the resistor for the overtone branch gets scaled as $Rn = R1 * n^2$, which implies that the negative resistance required to get oscillations on overtone is much larger than the value for fundamental mode. The fundamental frequency (lowest-mode) response is the most active due to lowest value of Rn. If a large negative resistance is provided for the fundamental resonance, it could result in exciting an overtone mode also. For designing high frequency crystal oscillators, generally the crystal is excited on its overtone mode and care should be taken to suppress the unwanted fundamental resonance in such cases.

Apart from the spurious resonances, the cut of the quartz resonator changes the angle of the crystalline orientation that leads to change in crystals behavior over the temperature. The temperature behavior is modeled by a third order polynomial of the form $\frac{\Delta f}{f} = a(t - T0) + b(t - T0)^2 + c(t - T0)^3$, where T0 is the inflection temperature [1], at which the change in frequency is minimum.

General examples of frequency changes over temperature, generally referred to as FT behavior observed in the range of -50^0c to $+125^0$c are shown in the figure (6) and figure (7). The FT behavior shows the crystals upper and lower turning points along with the inflection angle. To minimize the frequency changes resulting from temperature the oven of the OCXO is adjusted to the turning point of the crystal. Note for an AT cut crystal of 9 minutes, shows frequency change of about ±30ppm and inflection angle at 27^0c while an SC cut crystal of 9 minutes, shows the inflection angle around $+100^0$c with the changes in frequency from -225ppm to +50ppm.

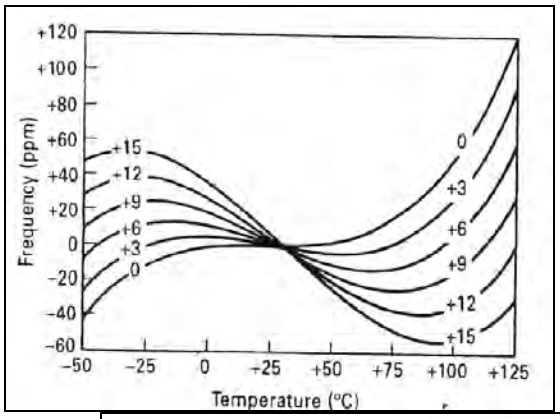


Figure 6: FT for AT cut resonators

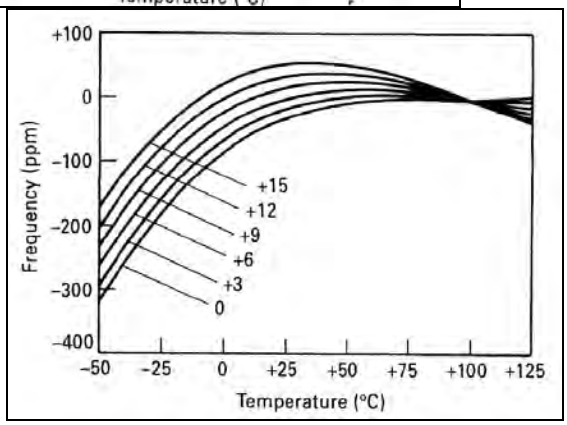


Figure 7: FT for SC cut resonators

In an SC cut and IT cut resonators the change in frequency is more towards the cold end but tend to flatten out as the temperature approaches the inflation angle as shown in figure (8). This makes them very suitable for Oven controlled oscillators where the temperature of the oven is set to the turn temperature. The AT cut on other hand has inflection angle around 27^0c, and that makes it suitable for TCXO application.

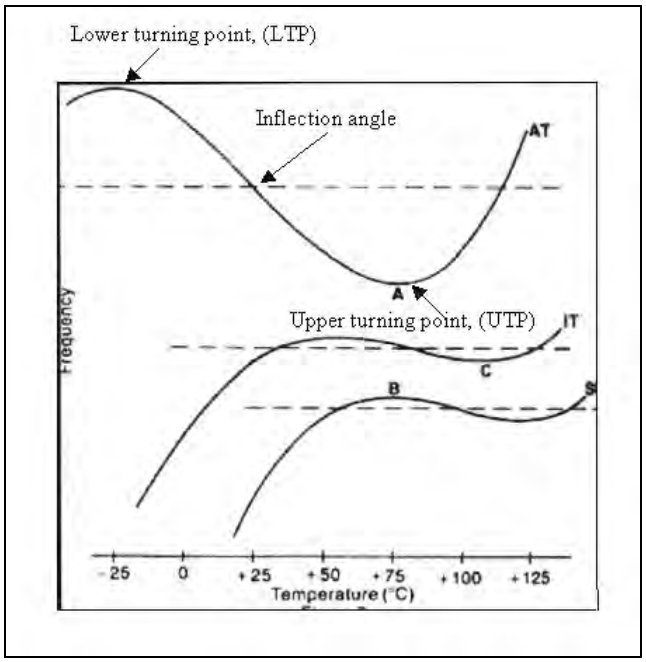


Figure 8: FT for AT cut, SC cut, IT cut resonators showing UTP, LTP and inflection angle.

The frequency variations in AT cut resonator are dependent on temperature and the thermal gradient of temperature across the crystals surface, where as the SC cut is immune to the thermal gradients. Since SC cut is nearly insensitive to the thermal gradients that invariably occur during oven warm-up, it is expected that SC cut resonators will give much faster warm-up in ovenized oscillators. The packaging and the control circuitry play a critical role in warm-up time of ovenized crystal oscillator.

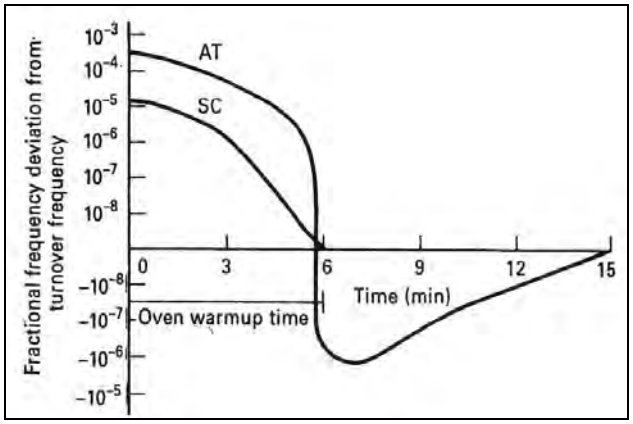


Figure 9: Typical warm-up for AT and SC cut oven oscillators

Another property of crystal is aging. This is strongly affected by cleanliness of the resonator and enclosure. A thin resonator is more affected of low aging by thin film of contamination than a thicker resonator. Also stress relaxation of the mount

structure and electrodes, excessive crystal drive power and out-gassing of materials in crystal support structure and electrodes contribute towards aging.

The commonly used crystal oscillators based on the compensation techniques are:

OCXO (Oven Controlled Crystal Oscillator): In OCXO the crystal and other temperature sensitive components are placed in a stable oven, which is adjusted to the temperature where the crystal's FT characteristics has zero slope. This is achieved by setting the oven temperature to either the LTP (lower temp) or UTP (upper temp), where the FT variations of the crystals are minimum. OCXOs can provide a >1000X improvement over the crystal's f vs. T variation. This can help in achieving stringent frequency stability as compared to a basic crystal oscillator design. These normally involve SC cut crystals.

TCXO (Temperature Compensated Crystal Oscillator): The temperature stability of the basic oscillator can be improved by incorporating the inverse temperature characteristics to nullify the FT of crystals. This type of crystal oscillators prefers to use AT cut crystals. Based on the circuit involved in its design TCXOs are categorized into two different types. One that employs a microcontroller is DTCXO, Digital TCXO and the other circuit uses thermistor network to control the temperature circuit termed just as TCXO or ATCXO, Analog TCXO. The technique employs a thermistor network and varactor in series with the crystal. Over the temperature the thermistor network would generate a voltage, which will be the inverse characteristics of the crystal. This voltage is applied across the varactor, which changes the capacitance in series with the crystal to bring it back to desired frequency. The stability requirements of most TCXOs dictate compensation by means of a multiple thermistor network with several interdependent variable components thus making the solution of simultaneous equations by computer the only feasible approach to temperature compensation. When the temperature compensation has stringent requirements then instead of the thermistor, it is preferred to use an ASIC or microcontroller based design, in which the microcontroller is programmed to generate the inverse FT response.

VCXO (Voltage Controlled Crystal Oscillator): These oscillators include a varactor diode in the circuitry, which allows frequency to be tuned to slightly different values. It can further be either temperature compensated (called TCVCXO) or Oven controlled (called OCVCXO) for better performance.

In general the floor of the TCXO's can be an almost as good as high stability ovenized oscillator, but the close-in phase noise and short-term stability are very poor relative to oven. This is because of the need to pull the oscillator frequency of a TCXO mandates a low resonator Q relative to an ovenized oscillator. The digital compensation of TCXO is constrained to not more than ±0.05ppm by the limitations of effects such as hysteresis in the frequency/temperature characteristics of the crystal and the adjustments required compensating for aging.

In broad view there should be 5 specifications for a crystal oscillator as follows:

Define Type of Oscillator	Attach Reference documents	Mention following Electrical Properties	Environmental Properties	Quality Assurance
TCXO VCXO OCXO etc..	Tests to be performed Testing methods Miltary Specifications if any etc..	Nominal Frequency ± Tolerance (ppm/0c) Output power and type of output Supply voltage ± supply tolerance Supply current ± current tolerance Tunning Range Warmup conditions Supply sensitivity Load sensitivity Phase noise and/or Allan variance Aging (per day, per year etc..) Radiation, accelaration sensitivity Magnetic field sensitivity	Temperature range operation storage Vibration Shock	any other test required that add upto the cost of unit Special markings etc..

A modern design approach for crystal oscillators using different circuits :

Certain requirements were set-forth to be fulfilled from this design. The main objective was to design a 10MHz crystal oscillator , one example with low phase noise, an output power of 10dBm with a voltage supply of 10 to 12 V and the load resistor is assumed to be 50 ohms.

For the first example the operational frequency is 10MHz, and the semi-isolated colpitts configuration is selected for the design. The Colpitts configuration is generally good for crystal oscillator design and good performance up to 50MHz and is also very simple to design. With the semi-isolated configuration, the output is taken from the collector that has higher ratio of output power level to crystal power. Changing the biasing component values but still maintaining the same output current we will be able to change the performance of phase noise [5, pp230].

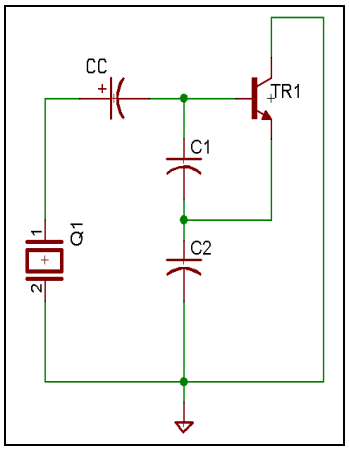


Figure 1: Basic Colpitts crystal oscillator

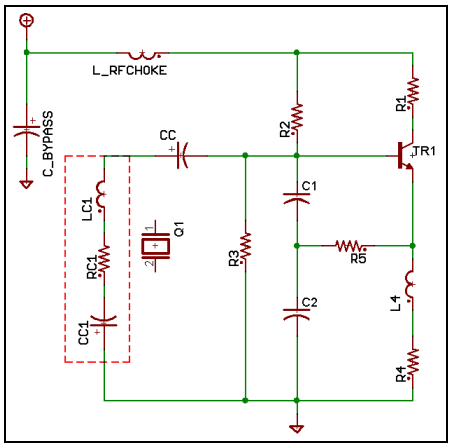


Figure 2: Colpitts oscillator—Crystal replaced with its equivalent schematic

To proceed through the design procedures and to calculate the values of each component, replace the crystal with its LC equivalent circuit and Q specified in the schematic as shown in figure 2. The first step in the design process involved calculating the operating point for fixed normalized drive of x=20 (table 6-1 from reference [5]). The output voltage $V_{out}(\omega_0)$ and current $I_{out}(\omega_0)$ at the fundamental frequency based on the output power requirements can be computed with following equation from ref. [5].

$$V_{out}(\omega_0) = \sqrt{P_{out}(\omega_0) * 2R_L} = \sqrt{0.01 * 2 * 50} = 1V$$

$$I_{out}(\omega_0) = \frac{V_{out}(\omega_0)}{50} = 20\,mA$$

$$where,\ output\ Power\ \left(P_{out}(\omega_0)\right) = 10dBm = 10mW$$

The DC operating point is calculated based on the normalized drive level x=20. The expression for the emitter dc current, $I_E(\omega_0) = I_{out}(\omega_0)$, can be found in terms of the Bessel function with respect to the drive level as (Ref. [5]).

$$I_E(\omega_0) = 2I_{DC}\left[\frac{I_1(x)}{I_0(x)}\right] \Rightarrow I_{DC} = 10.26mA$$

The NEC transistor BFP193 was selected and biased as shown in figure 3. The resistor values were determined such that they satisfy our requirements of 10V supply and 10mA current.

$$Assume \quad Vce = 4.2\ v$$

$$\beta = 100$$

$$Ve = 4.7\ v$$

$$Ie = Ic + Ib$$

$$Ib = \frac{Ic}{\beta} = \frac{10\ mA}{100} = 0.1\ mA$$

$$\therefore Ie = 10.1\ mA$$

$$Ve = Ie * R4$$

$$\Rightarrow R4 = 465.3\ \Omega \approx 470\ \Omega \quad std$$

$$R1 = \frac{Vcc - (Ve + Vce)}{Ic} = 100\ \Omega \quad std$$

$$Vb = 5.4\ v = \frac{Vcc * R3}{R3 + R2}$$

$$\Rightarrow \quad R3 = 15\ K\Omega \quad if \ \ R2 = 10\ K\Omega$$

The circuit with calculated values was simulated in Ansoft designer for DC analysis and the currents and voltage verified. The third step involves calculating the large-signal transconductance Y21 parameter from the table 6-1 and 6-2 in reference [5].

$$Y_{21}\big|_{lg} = G_m(x) = \frac{qI_{DC}}{kTx}\left[\frac{2I_1(x)}{I_0(x)}\right]_{f=fundamental}$$

$$\left[Y_{21}\right]_{\omega=\omega_0} = \left[\frac{1.949 I_{E-DC}}{520mV}\right] = 50.83mS$$

Here the term $Y_{21}\big|_{lg}$ is the large signal transconductance.

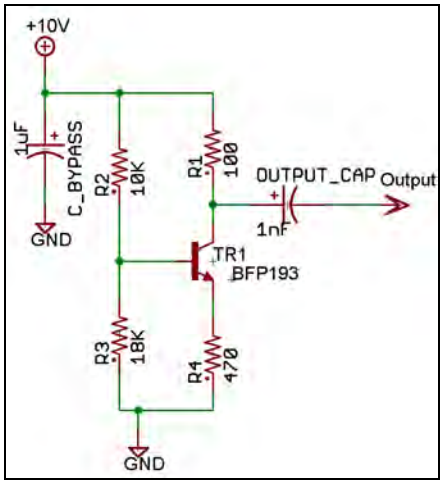


Figure 3: Fixed biasing for bipolar transistor BFP193

The transformation factor *n* is calculated based on the quadratic equation and the large-signal transconductance parameter of transistor BFP193 [5,Ch 6]. The value of n is selected from the set of n1 and n2, both inclusive, for a given drive-level, x=20.

$$n^2(G2+G3)-n(2G3+Y21\alpha)+(G1+G3+Y21)=0$$
$$\Rightarrow n1=17.2581 \quad and \quad n2=1.0251$$
$$Let \quad n=2$$
$$C1=58.9\,pF \quad and \quad C2=58.9\,pF$$
$$Cc=33\,pF$$
$$Ceff=\frac{Cc*C1*C2}{C2*Cc+C1*Cc+C1*C2}=15.576\,pF$$
$$Leff=86.878uH$$

The values calculated are for the circuit in figure 2. C1 and C2 are the capacitors in capacitive feedback network, while Cc is the coupling capacitor. The *Leff* , is the effective inductance required to form oscillations. The above circuit oscillates with a lumped inductor of value *Leff* and the phase noise is not so good due to the assumption of less Q for the resonator while, the output frequency of the circuit as revealed by the non-linear analysis from serenade program is 9.242MHz.This exercise was done to harmonize that a Colpitts oscillator needed an inductor or inductive resonator with the capacitive divider feedback to form oscillations. The above design values give a reliable preparatory point to further optimizing the design. The values of Q (defined by Rc1), Lc1 (Lc1= *Leff* as initial design step) and Cc1 (initial value computed such that $XLc1+\frac{1}{XCc1}=0$) in figure (2) are then scaled and tuned to match the crystal parameters to be used. In general the inductance of the crystal is in few Henrys and the capacitance is in few Femto-Farads while the Q of the crystal is a few millions.

We have assumed the value of transformation factor, $n=2$, which require that the design have feedback capacitors of 59pF, this can be further optimized to get the minimum phase noise. The value of n, transformation factor is varied for optimum phase noise and output power and is generally computed from the derivative of the phase noise equation, as shown in Ref. [5], and written the following form [5, pp181],

$$\frac{\partial}{\partial y}\left\{\left[k0+\left(\frac{k^3k1\left[\frac{Y_{21}|_{lg}}{Y_{11}|_{lg}}\right]^2 y^{2P}}{Y_{21}|_{lg}{}^3\, y^{3Q}}\right)*\left(\frac{1}{y^2+k}\right)\right]*\left[\frac{(1+y)^2}{y^2}\right]\right\}_{y=m}=0$$

where, $Y_{21}\big|_{lg}$ is the large signal transconductance and $Y_{11}\big|_{lg}$ is the large signal admittance.

$$k0 = \frac{\kappa TR}{\omega^2 \omega_0^2 L^2 V_{CE}^2 C_2^2}$$

$$k1 = \frac{qI_c gm^2 + \left(K_f \frac{I_b^{A_f}}{\omega} \right) gm^2}{\omega^2 \omega_0^2 L^2 V_{CE}^2}$$

$$k2 = \omega_0^4 \beta^2$$

$$k3 = gm^2 \omega_0^2$$

$$k = \frac{k3}{k2C_2^2} \Rightarrow C_2^2 = \frac{k3}{kk2}$$

$$y = \frac{C_1}{C_2}$$

Here, K_f is the flicker noise coefficient, *AF* is the flicker noise exponent, *R* is the equivalent loss resistance of the tuned resonator circuit, I_c is the RF collector current, I_b is the RF base current, V_{CE} is the RF collector voltage, C_1, C_2 is the feedback capacitor, *P* and *Q* are the drive level dependent constant across base-emitter of the device. From curve-fitting attempts, the following values for *P* and *Q* were determined (*P* =1.3 to 1.6; *Q* =1 to 1.1).

The simulation for different values of n and the C1, C2 computed for that value of n shows the following phase noise and output power results. A lower value of n can be opted at the cost of increased harmonic outputs.

n	C1 (pF)	C2 (pF)	dBc/Hz@ 10Hz	dBc/Hz@ 100Hz	dBc/Hz@ 1KHz	dBc/Hz@ 10KHz	dBc/Hz@ 100KHz
1.10	33	330	-117.5	-128.0	-138.1	-148.0	-157.8
1.20	36	180	-120.9	-131.0	-141.0	-150.9	-160.5
1.30	39	124	-116.7	128.9	-138.9	-148.8	-158.5
1.35	39	110	-114.3	-128.5	-138.6	-148.5	-158.2
1.40	42	100	-112.0	-127.6	-137.5	-147.7	-157.2
1.50	47	82	-108.2	-126.7	-136.5	-146.5	-156.2
2.00	59	59	-100.8	-127.6	-137.0	-147.0	-156.6
2.50	75	47	-95.4	-125.4	-140.0	-150.0	-159.8
3.00	82	47	-97.9	-127.8	-139.0	-149.4	-159.0
4.00	110	39	-94.6	-124.6	-141.8	-151.7	-160.9

The design is almost complete. We may need some additional filtering components to filter out the harmonic contents for the circuit. The harmonic contents are function of drive level. As the drive level increase the harmonic contents also increase and additional filtering is required for the proper suppression of harmonic contents. We can now compute the noise factor and the phase noise of the system from all the components values. We use the following equation to compute the noise factor for the oscillator from ref.[5 pp. 133].

$$F = 1 + \frac{Y_{21}|_{lg} C_2 C_C}{(C_1 + C_2) C_1} \left[r_b + \frac{1}{2 r_e} \left[r_b + \frac{(C_1 + C_2) C_1}{Y_{21}|_{lg} C_2 C_C} \right]^2 \left[\frac{1}{\beta|_{lg}} + \frac{f_0^2}{f_T^2} \right] + \frac{r_e}{2} \right]$$

where, r_b is the base resistance, $r_b = 7.2326\Omega$ while r_e is the emitter resistance of the transistor $r_e = 1.0075\Omega$ and f_T is the transition frequency for the transistor $f_T = 5GHz$. The large signal current gain is given as $\beta|_{lg} = \frac{Y_{21}|_{lg}}{Y_{11}|_{lg}} \left(\frac{C_1}{C_2} \right)^P$.

The mathematically computed value for noise factor is 2.0016 and the noise figure for the oscillator given as $noiseFigure = 10 * \log 10(F)$ was computed to be 3.01385dB for transformation factor, n=2.

The final step in the approach is to calculate the phase noise from the following equation of ref [5, pp.131 equation; 7-26]

$$L(f_m) = 10 \log \left\{ \left[1 + \frac{f_0^2}{(2 f_m Q_L)^2} \right] \left(1 + \frac{f_c}{f_m} \right) \frac{FkT}{2 P_{sav}} + \frac{2 kTRK_0^2}{f_m^2} \right\}$$

where, Q_L is the loaded Q factor of the oscillator, F is the noise factor, kT is Boltzman's constant, R is the equivalent loss resistance of the tuned resonator circuit or equivalent noise resistance of tuning diode (typically 50Ω -10kΩ), and P_{sav} is the average power at oscillator output, K_o = voltage gain. The phase noise of the system has been determined theoretically and agrees with simulated response from Ansoft Serenade [6]. The figure (4) and figure (5) below shows the phase noise and the output power plot from the Serenade program.

f_m	1Hz	10Hz	100Hz	1000Hz	10KHz	1
Phase noise	-66.85	-96.18	-121.44	-137.68	-147.65	-

The calculated phase noise (shown in the table) for offset frequency f_m from the carrier frequency f_0 agreed closely to the simulated values (shown in figure 4).

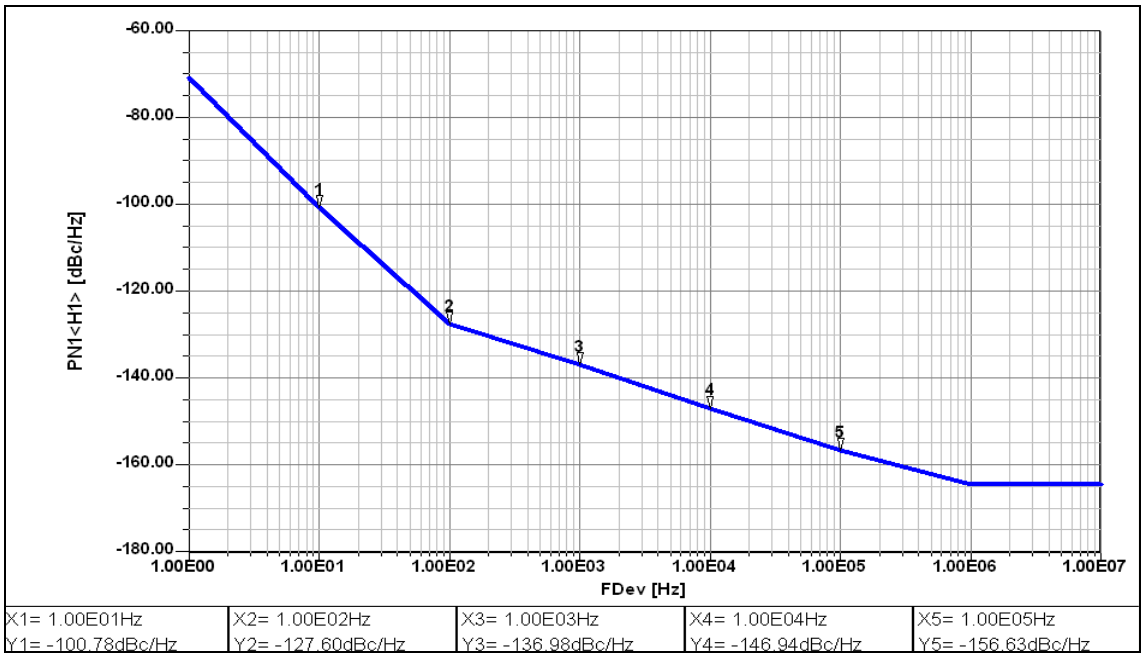


Figure 4: Colpitts oscillator—Phase noise with C1=59pF and C2=59pF

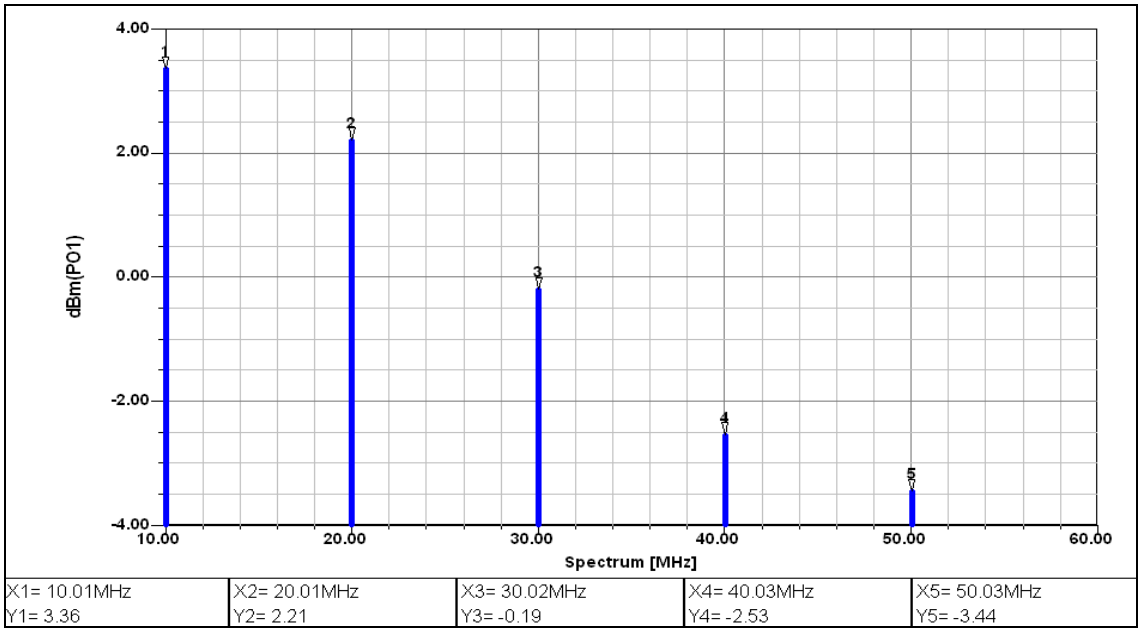


Figure 5: Colpitts oscillator—Output power

Since quartz crystal is mechanical resonator driven by the piezoelectric effect, fundamental and a variety of overtone frequency modes are possible. Unfortunately undesired mode jumping is also possible even in well-planned circuit designs. This problem can be overcome by mode feedback mechanism that not only improves the stability but also improves the phase noise performances by few dB. The feedback resistor R5, which is generally a short at high frequency, gives better performance of phase noise than in a circuit otherwise, assuming there is no flicker noise in the crystal. The complexity on feedback resistor can be

instituted in [3] and [4]. The dynamic mode feedback approach is introduced in reference [3] that includes a methodology for optimum coupling to enhance the dynamic loaded Q, and to reduce or eliminate phase hits, while reducing the thermal drift and susceptibility to micro phonics to an extremely low level, and retaining low phase noise and broadband tunability. A mode feedback coupling is a method in which the crystal is operated in its overtone mode, say the 3rd overtone and then a signal with same amplitude and phase as the 3rd overtone is injected in the resonator such that certain features are canceled and a get better phase noise is obtained.

The adjoining figure show the schematic with the feedback resistor been identified and the change in phase noise due to presence of the resistor as compared to its absence. The presence of the feedback resistor reduces the negative impedance presented by the transistor to the resonator. So the values of the capacitive feedback network can be adjusted in order to set the oscillations.

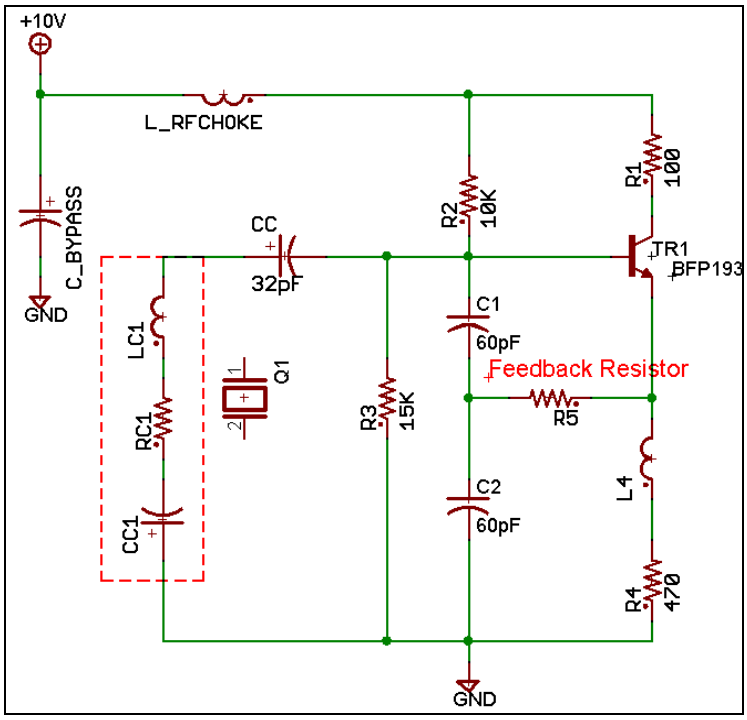


Figure 6: Feedback Resistor

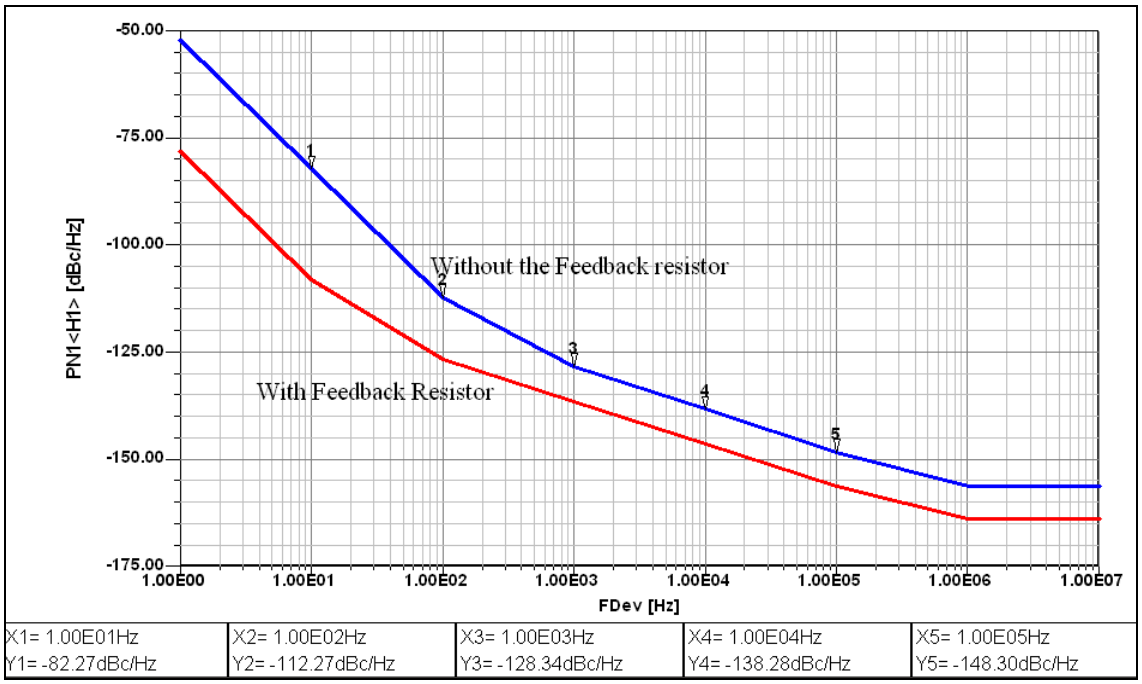


Figure 7: Phase noise of the circuit with and without the feedback resistor.

There are different ways to improve phase noise and the biasing current is one of them. Not only does the proper current will change the phase noise of the oscillator but also the best biasing techniques. We found that given the same current and supply voltage, transistor with fixed biasing gave better results over self-biasing techniques. The voltage feedback form of the stabilized biasing network, or self-biasing technique shown in figure (8), provides voltage feedback to the bias current source resistor RBASE. The base current source is fed from the voltage across the collector-emitter of the transistor V_{ce}, as opposed to the supply voltage V_{cc}. The collector resistor has both I_c and I_b flowing through it The variation in β_{dc}, due to change in the temperature will cause changes in the collector current I_c. Any increase in voltage across R_c will cause V_{ce} to decrease, and this will cause I_b to decrease because the potential difference across the base resistor R_B is decreased. This configuration of the biasing circuit provides negative feedback that tends to reduce the amount by which the collector current increase as β_{dc} is increased due to the rise in temperature, ref [5 pp 219].

$$Ic = \frac{\beta_{DC}\left(V_{CC} - V_{BE}^{'}\right) + I_{CBO}\left(1+\beta_{DC}\right)\left(h_{ie} + R_B + R_C\right)}{h_{ie} + R_B + R_C\left(1+\beta_{DC}\right)}$$

All three temperature-dependent variables, β_{dc}, I_c and V_{ce} influence the collector current due to change in temperature, the derivative of I_c with respect to each factor gives the stability factor for the biasing circuit.

The emitter feedback bias network as in figure (8), where a resistor is connected in series with the device emitter lead to provide the voltage feedback, provides an optimum control over variations in β_{dc} due to variations in temperature and also

from device to device. The emitter resistor must be properly RF bypassed to avoid regenerative effect.

Our example from figure (8) has fixed biasing or the emitter feedback biasing technique. The same circuit was modified to use the voltage feedback biasing of stabilized biasing or the self-biasing technique as shown in figure (8). Both the biasing provided the same collector current of 9.8mA to the oscillator.

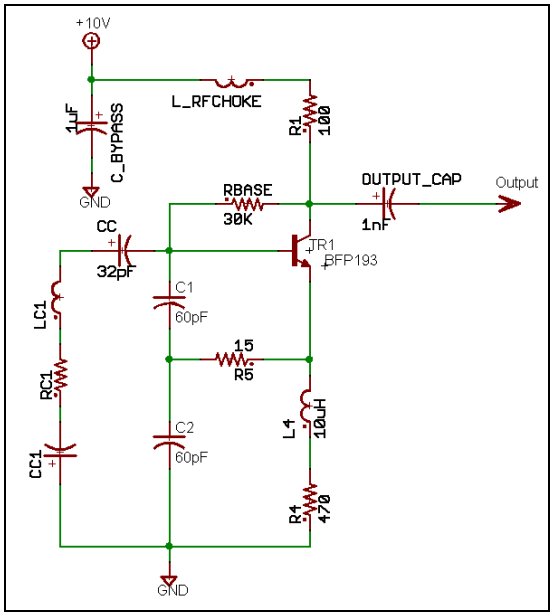


Figure 8: Self biasing for the transistor

The phase noise of the fixed biasing was found to be much better in the close in than that obtained with self-biasing (shown in figure 9).

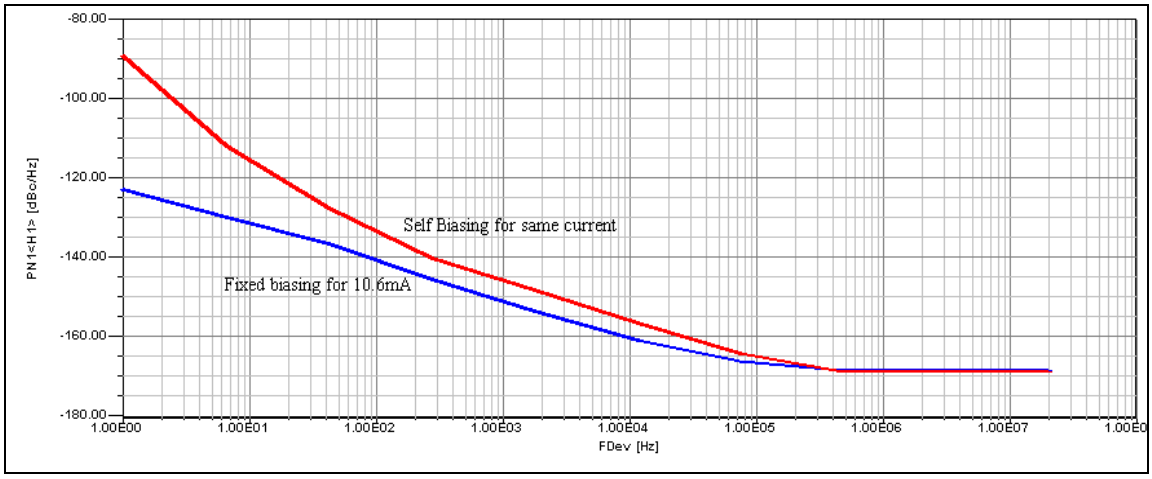


Figure 9: Phase noise comparison between the fixed biasing and the voltage feedback biasing techniques for the transistor.

For further validation silicon N-channel FET based colpitts oscillator was designed with the same current as in the previous example of figure (8). Figure (10) shows the circuit diagram for the FET based oscillator. Traps in the gate-channel depletion layer, traps in the substrates and possibly surface states created by the passivation cause the noise is FET, Ref [7, pp.175]. Much higher 1/f noise occurs in MOSFETs because of the traps in the oxide. Since the noise is voltage noise it is generally plotted as dBv/√Hz. It is found that the BJT has a superior much lower corner frequency, f_c. The GaAs MESFETs will dominate the microwave region but the silicon BJTs will continue to find applications especially for low noise oscillator.

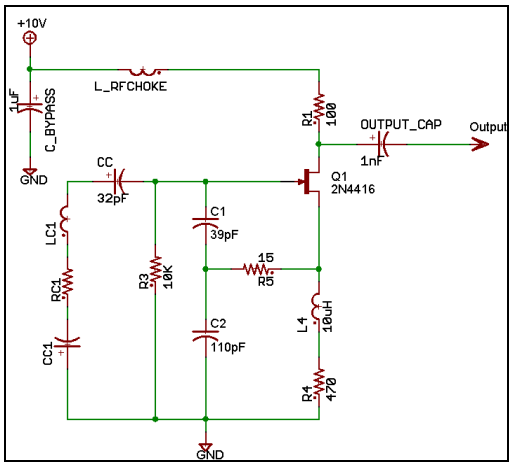


Figure 10: FET oscillator similar to figure (8), same biasing current.

We studied that FET improved the phase noise under same biasing conditions for our example of 10MHz Colpitts oscillator. The output frequency obtained from the BJT was 10.00682MHz and was shifted to a high side when a FET was used. The figure (11) shows the phase noise comparison of using a FET over the BJT for this particular application.

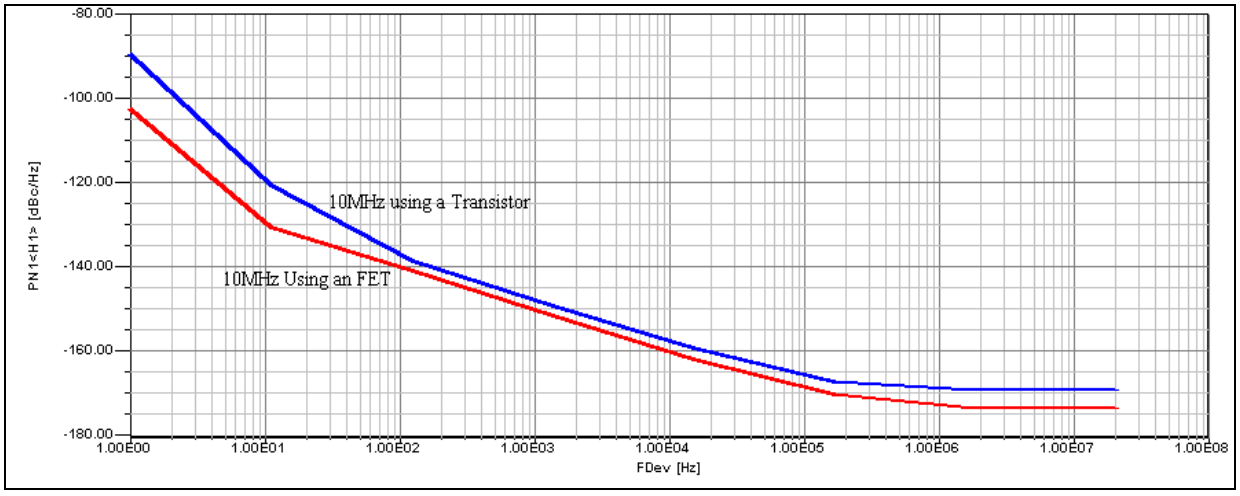


Figure 11: Comparison between using a transistor and FET

A practical circuit was built as per the above design guidelines in Colpitts oscillator configuration. When measured with the circuit values, as shown in figure (12) with the crystal used from Bliley showed a comparable response. The bias was changed and the output stage was connected to amplifier while doing the measurements. The amplifier or the buffer stage of FET does not load the circuit because of the infinite impedance of the FET. The dual gate MOSFET's are the best choice for buffer stage. The simulated results agreed with the measured data. The difference in the phase noise at higher end is due to use of amplifier while measurements. The noise figure of the amplifier raises the noise floor as shown in the simulation plot.

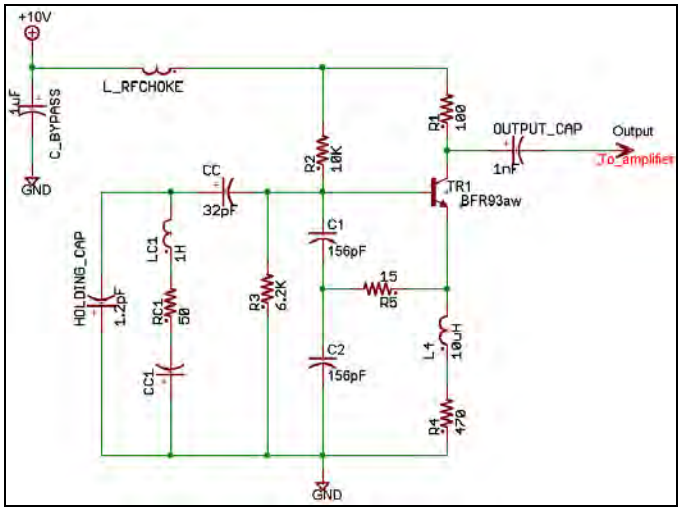


Figure 12: Circuit for of 10MHz oscillator without the Amplifier at the output.

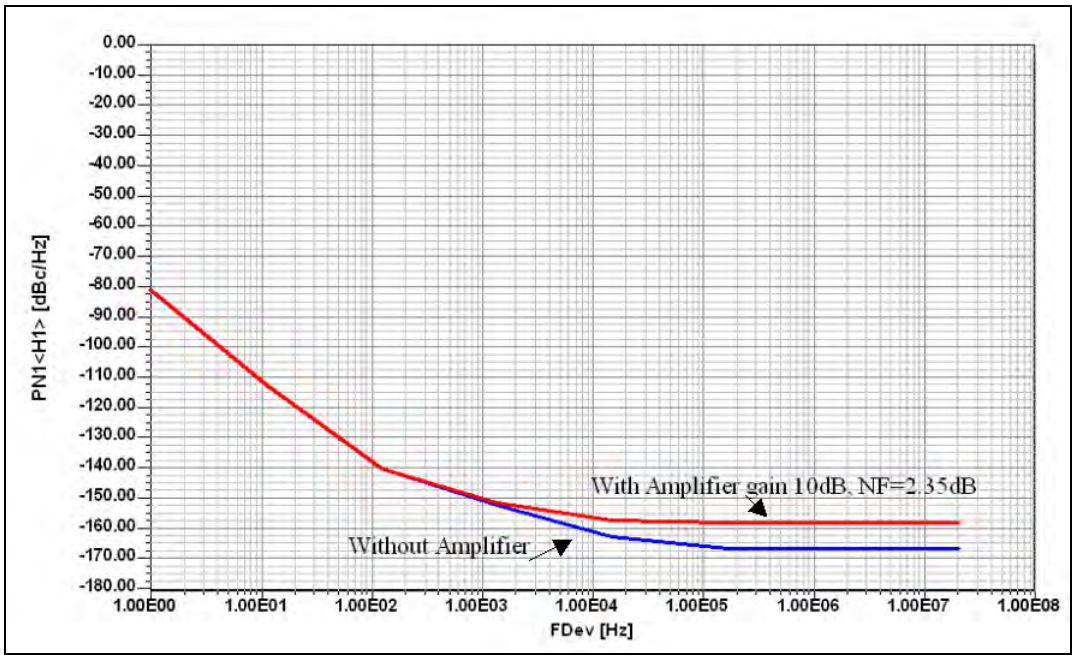


Figure 13: Simulated phase noise of the 10MHz oscillator from figure (12), with and without amplifier at the output, using the Serenade program.

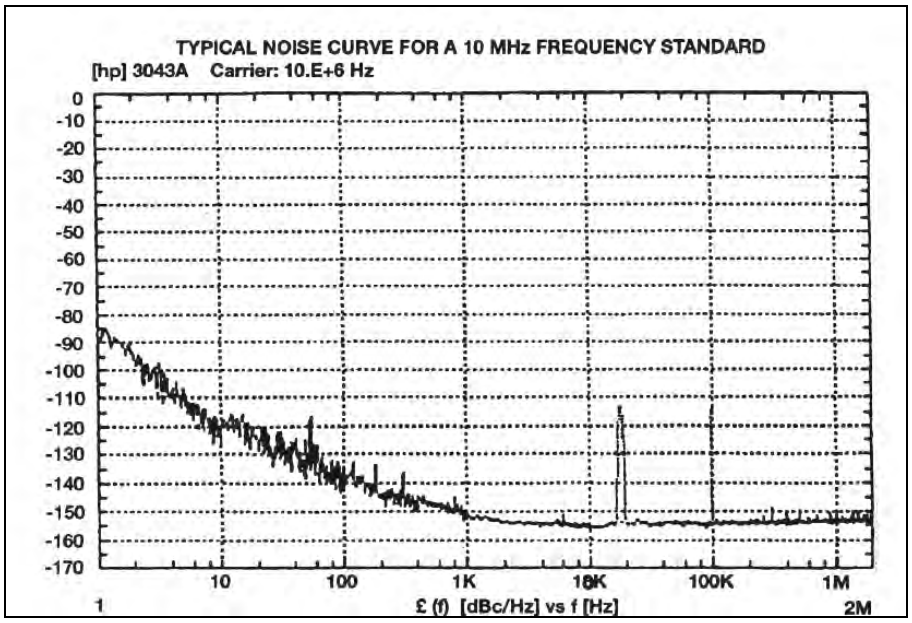


Figure 14: Measured phase noise of the 10MHz oscillator.

Assortments of modifications to the Pierce and Colpitts oscillator are studied in the following section. These modifications are to achieve certain advantages (along with its unwanted disadvantages) over the standard configuration. Shown below is the semi-isolated Colpitts oscillator. Due to coupling of load through Cc, this circuit is not recommended for frequencies above 10MHz at fundamental operational frequency. This limitation of frequency range is due to the miller capacitance at high frequencies. This circuit can be used if instead of the fundamental mode we have an output from the overtones. Characteristics in oscillator also depend from where the output is tapped out. In the normal Colpitts configuration we take the output from the emitter of the transistor. Since there is no collector resistor in the typical Colpitts configuration, the limiting is due to cutoff in transistor. In the normal oscillator the power extracted from the load is much less than the crystal power. More power is extracted only at the expense of loaded Q.

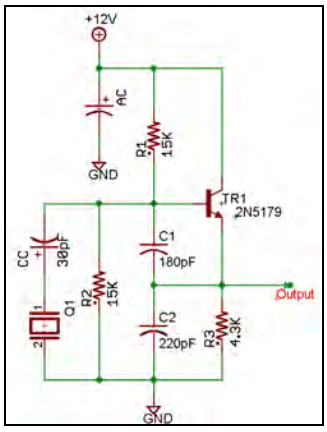


Figure 15: Colpitts oscillator, output from emitter.

In the above examples Figure 12 and Figure 8, and the following two, the output is taken from the collector; such configuration is called the semi-isolated Colpitts configuration. The principal advantage of this configuration is larger output power as compared with the crystal power and better isolation to load than the normal Colpitts configuration. By tuning the collector to harmonic of the oscillator frequency, the circuit acts as frequency multiplier, which gives additional isolation from load to oscillator. Figure (16) is a semi-isolated Colpitts configuration in which a 3.333MHz oscillator gives a tuned output frequency of 10MHz.

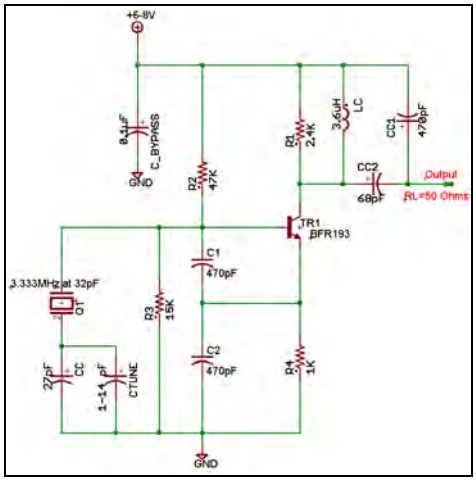


Figure 16: Semi-isolated Colpitts configuration for 10MHz

The output of the semi-isolated Colpitts oscillator can be DC coupled into a common base amplifier in a cascode arrangement. This modification gives excellent isolation to the load and allows much larger collector load in the second transistor. By changing the configuration of the crystal the output current can be forced to flow through the resonator, which reduces the noise floor considerably.

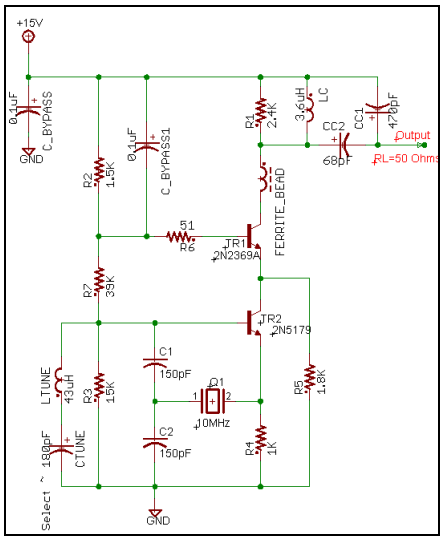


Figure 17:Modified Semi-isolated Colpitts, 10MHz oscillator in Cascode configuration.

Another example of the Colpitts oscillator is the configuration in which the power is extracted from the resonator, reference [20]. By extracting the resonator power from crystal the crystal acts as a very narrow band filter on noise generated by the oscillator stage. A schematic with FET operating for 5MHz operational frequency is shown in figure 18.

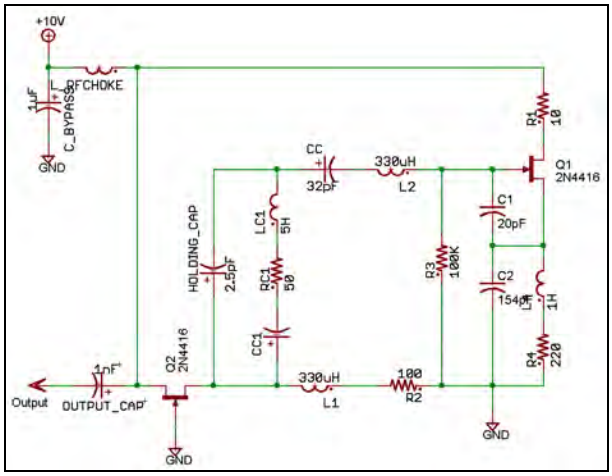


Figure 18: A Modified Semi-isolated Colpitts oscillator for 5MHz in which the power is extracted from resonator.

Since a common base stage has very low input impedance at the emitter, the Q degradation will be very slight. The principal disadvantage of this circuit is that the output power will be a small percentage of the crystal power. This may cause poor floor noise or high crystal power dissipation, but this configuration gives better harmonic rejection and good isolation.

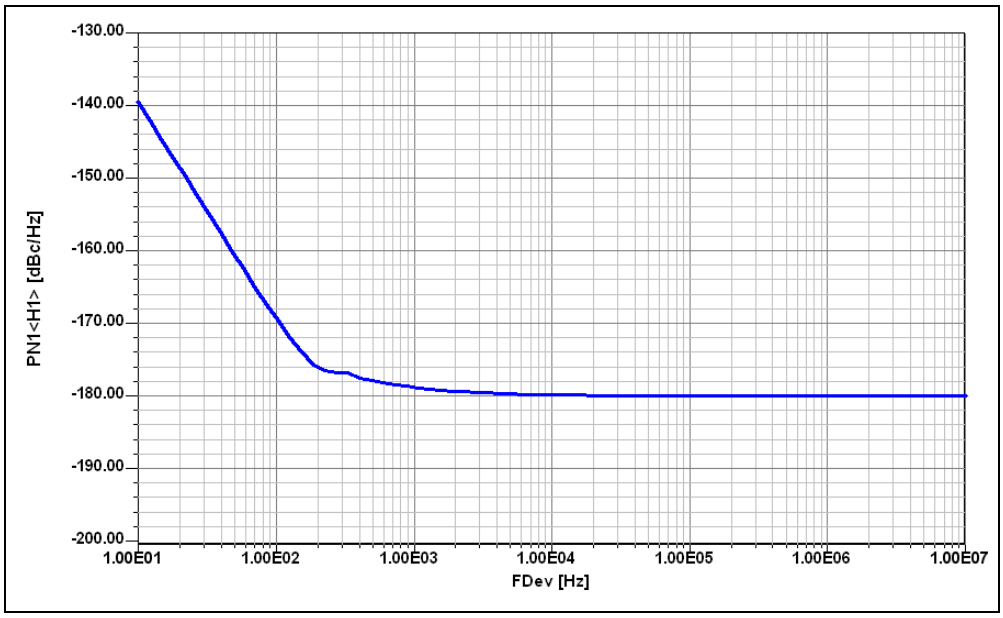


Figure 19: A Modified Colpitts oscillator with power extracted through resonator for 5MHz.

The noise parameter for FET was not considered.

Low-frequency crystals have thicker and large quartz wafers and ranges in few Henrys, whereas, high-frequency crystals have thinner and smaller quartz wafers and ranges in a few micro Henrys. Starting at about 30 MHz, the quartz becomes so thin that it is hard to handle during the manufacturing process. Inverted "mesa crystals" allow crystal to resonate at higher fundamental mode frequency (above 30 MHz) but manufacturing process is not cost-effective with respect to oscillator stability and phase noise performances.

The promising alternative is overtone mode, which is similar in concept to a harmonic, with the exception that crystal oscillation overtones are not exact integer multiples of the fundamental. An overtone-mode crystal cannot be used in a fundamental-mode oscillator, and vice versa, it may oscillate but not at the correct frequency and exhibit poor stability.

As an example, Figure 20(a), a 100 MHz crystal resonator based Colpitts oscillator was designed according to a set of specifications that included +13 dBm output power, 50-Ω load, and phase noise of –132 dBc/Hz offset 100 Hz from the carrier, with the intention of applying the new approach to this basic design to determine the component parameters that mostly affect the phase noise performance for a given class and topology. For this typical design example, an NE68830 transistor from NEC was selected for validation. Revising the design procedure for this particular design we have the following steps.

The first step in the design process involved calculating the operating point for a fixed normalized drive of x = 20, as described earlier. The output voltage and

current at the fundamental frequency (f_0, $\omega_0 = 2\ f_0$), based on the output-power requirement, can be given by

$$V_{out}(\omega_0) = \sqrt{P_{out}(\omega_0) * 2R_L} = \sqrt{20E - 3 * 2 * 50} = 1.414V$$

$$I_{out}(\omega_0) = \frac{V_{out}(\omega_0)}{50} = 28.3mA$$

$$\left[I_E(\omega_0)\right]_{x=20} = \left[I_{E1}(\omega_0)\right]_{x=20} + \left[I_{E2}(\omega_0)\right]_{x=20} = 2I_{DC}\left[\frac{I_1(x)}{I_0(x)}\right]_{x=20} \approx 56mA$$

$$\left[I_{E1}(\omega_0)\right]_{x=20} = I_{out}(\omega_0) = 28.3mA \text{ (O/P current to the load)}$$

$$\left[I_{E2}(\omega_0)\right]_{x=20} = \left[I_E(\omega_0)\right]_{x=20} - \left[I_{E1}(\omega_0)\right]_{x=20} = 27.3mA$$

$$I_{E-DC} = \frac{\left[I_E(\omega_0)\right]_{x=20}}{2\left[\frac{I_1(x)}{I_0(x)}\right]_{x=20}} = 28.3mA$$

The second step in the design process involved the development of the biasing circuit. For the best close-in phase noise, a noise-feedback DC circuit is incorporated to provide the desired operating DC conditions with I_E = 28.3 mA, V_{CE} = 5.5 V, supply voltage, V_{cc} = 8 V, $\beta \approx 120$, and $I_B \approx 0.23$ mA.

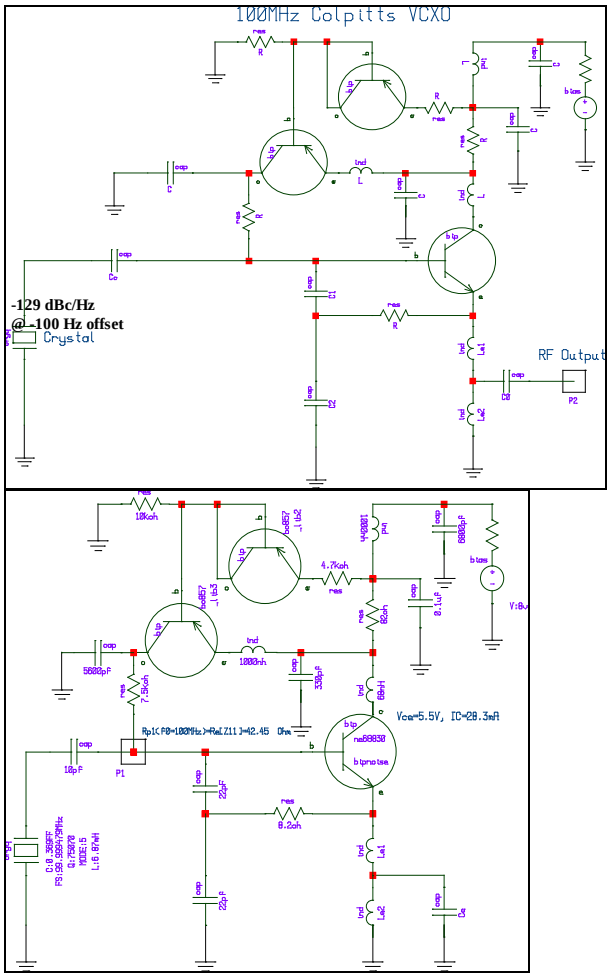


Figure 20: (a) 100MHz VCXO (tuning diodes and holder capacitance canceling inductance are missing for simplification), (b) Loss resistance R_{p1} (Port: P_1).

The third step involves calculating the large-signal transconductance Y_{21}

$$Y_{21}\big|_{\lg} = G_m(x) = \frac{qI_{DC}}{kTx}\left[\frac{2I_1(x)}{I_0(x)}\right]_{f=fundamental}$$

$$\left[Y_{21}\right]_{\omega=\omega_0} = \left[\frac{1.949I_{E-DC}}{520mV}\right] = 107mS$$

The fourth step in the procedure involves the calculation of loop gain and equivalent loss resistance as

$$Loop-Gain = [LG]_{sustained-condition} = \left[\frac{R_{p1}(f_0)Y_{21}(x)}{n}\right] = \left[\frac{Rg_m}{x}\right]\left[\frac{2I_1(x)}{I_0(x)}\right]\left[\frac{1}{n}\right] > 1$$

$$R_{p1}(f_0) = \mathrm{Re}[Z_{11}] = 42.45\Omega$$

where, $R_{p1}(f_0)$ is the equivalent resistive load across the port 1 (Figure 20b). For practical purpose, the loop gain should be 2.1 to achieve good starting conditions for stable and guaranteed oscillation.

$$n = \left[\frac{R_{P1}(f_0)Y_{21}(x)}{Loop-Gain}\right] = \frac{0.107\times 42.45}{2.1} \approx 2.16$$

The fifth step in the design procedure involves calculation of the feedback capacitor ratio based on transformation factor, n as

$$n = 1+\left[\frac{C_1}{C_2}\right] = 2.16 \Rightarrow \left[\frac{C_1}{C_2}\right]_{x=20} = 1.16$$

The sixth step involves calculation of the absolute value of the feedback capacitor based on the input impedance Z_{in} (looking into the base of the transistor). The expression for Z_{in} is given as

$$Z_{in} \cong -\left[\left(\frac{Y_{21}}{\omega^2(C_1^*+C_p)C_2}\right)\left(\frac{1}{(1+\omega^2Y_{21}^2L_p^2)}\right)\right] - j\left[\left(\frac{(C_1^*+C_P+C_2)}{\omega(C_1^*+C_P)C_2}\right) - \left(\frac{\omega Y_{21}L_P}{(1+\omega^2 ii Y_{21}^2L_p^2)}\right)\left(\frac{Y_{21}}{\omega(C_1^*+C_P)C_2}\right)\right]$$

where, C_P = (C_{BEPKG} +Contribution from layout)=1.1pF, L_P=(L_B + L_{BX} +Contribution from layout)=2.2nH. The expression for the negative resistance (R_n, without parasitic) can be described by

$$R_{neq} = \frac{R_n}{(1+\omega^2Y_{21}^2L_P^2)} \cong \frac{R_n}{1.0218}$$

$$R_n = -\left[\frac{Y_{21}^{+}}{\omega^2C_1C_2}\right]_{x=20} = \frac{0.107}{(2\pi\times 1\times 10^8)^2C_1C_2}$$

For sustained oscillation $\rightarrow$ Rneq $\geq$ 2RP1(f0) $\cong$ 84.9Ω

$$R_n \geq 1.0218\times 84.9 \cong 86.76\Omega$$

$$\therefore \quad C_1C_2 \leq \left[\frac{1}{(2\pi\times 1\times 10^8)^2}\right]\left[\frac{0.107}{86.76}\right] \approx 3.13\times 10^{-21}$$

$$C_1 = 25pF = [C_1^* + C_P] \Rightarrow C_1^* = C_1 - C_P = 23.84pF, \quad C_2 = 22pF$$

For practical purpose, C_1^*=22pF. The sixth step is to determine noise factor (F), which is needed prior for the evaluation of the phase noise and the final step in the approach involves calculating the phase noise.

The calculated phase noise at 100 Hz offset from the carrier frequency of 100MHz is –132 dBc/Hz (Q=100,000).

Figure-20 incorporates the component values as per above design calculations and figures 21 and 22 shows the simulated phase noise and output power for 100 MHz crystal oscillators. Simulated and calculated data of the oscillator agrees within 2-3dB.

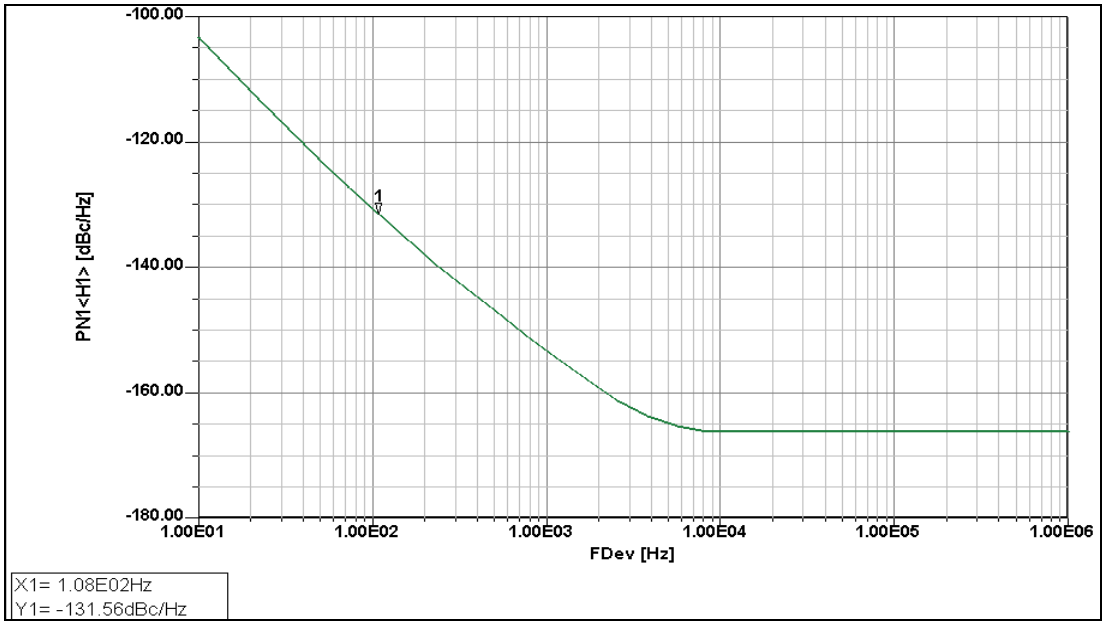


Figure 21: Simulated phase noise plot of 100MHz VCXO

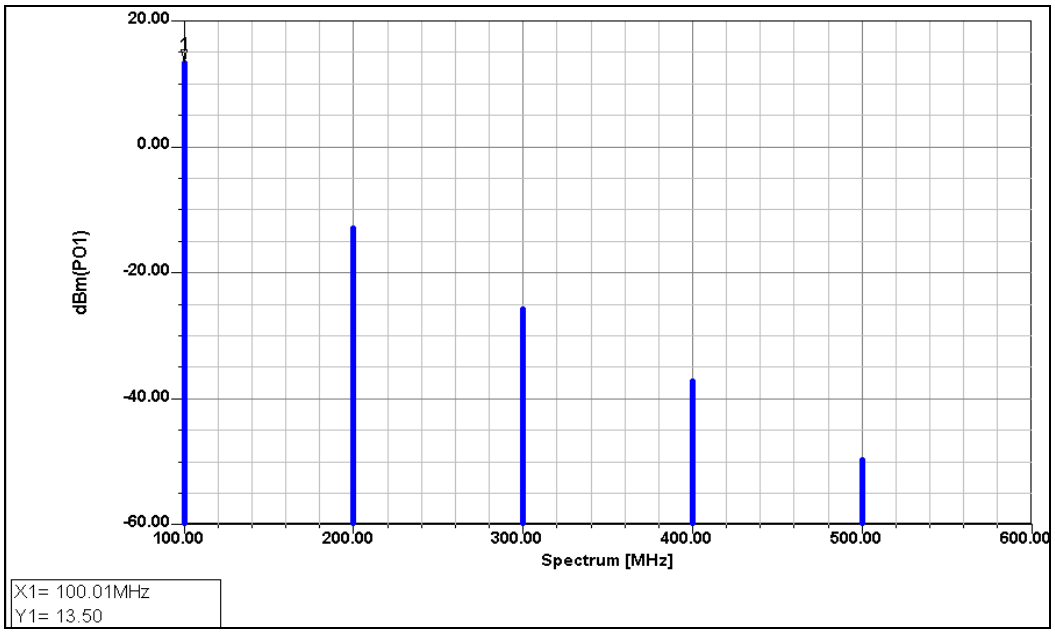


Figure 22: Simulated O/P power plot of 100MHz VCXO

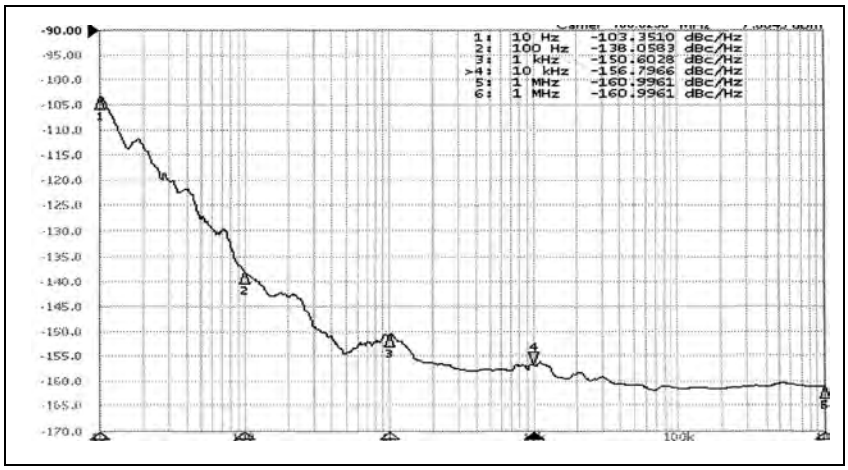


Figure 23: Measured phase noise plot of 100MHz VCXO

A Butler oscillator, or the bridged-T oscillator, is the most popular member of a family of oscillators where the emitter current is the current through the resonator, or crystal. As the current flows through the crystal it is much sinusoidal and the harmonic contents are reduced to a large extent. This filtering action improves the phase noise outside the effective bandwidth of the crystals, resonant frequency, f, by operating Q.

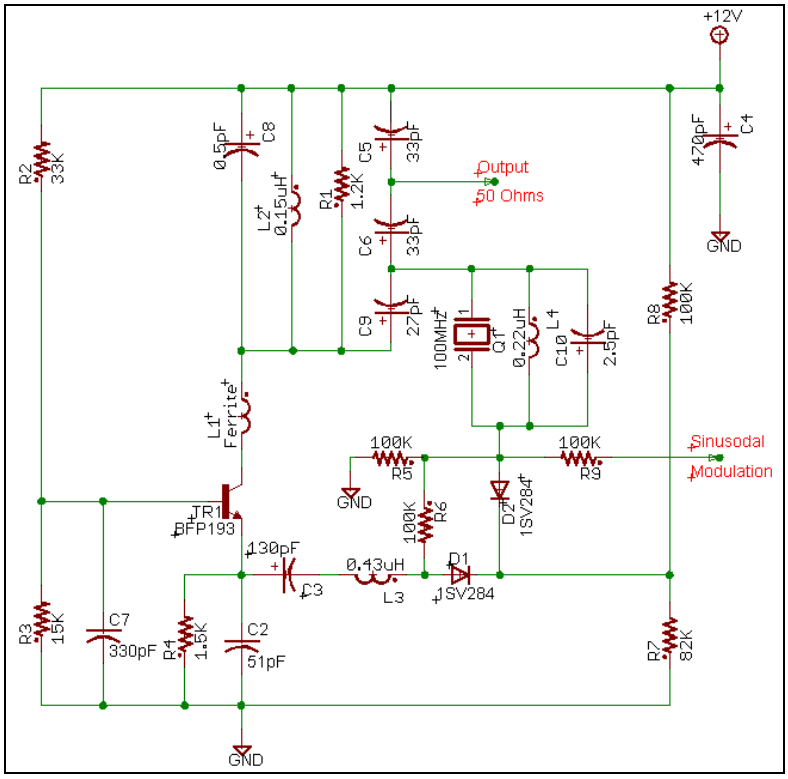


Figure 24: 100MHz 5th Overtone oscillator in Butler Configuration

The circuit in figure 24 shows a design of a 5th overtone 100 MHz crystal oscillator. In this case, the collector impedance for the other responses is very low, and the oscillations can be sustained only at the fifth mode.

The crystal holding capacitor *C0* is tuned out by L4 (0.22uH inductor in figure 24) is used to tuned out any spurious oscillations that can occur. This also greatly improves the voltage linearity of the output response. The circuit is forced to the desired output frequency by the collector tank for any susceptible oscillations, if any.

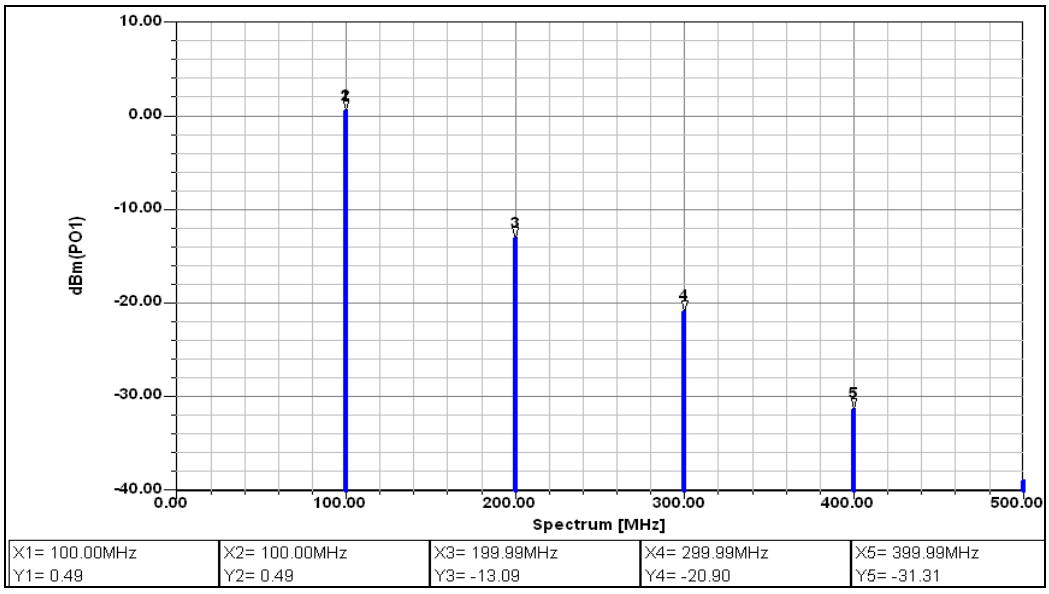


Figure 25: Output of 100MHz 5th overtone Butler oscillator

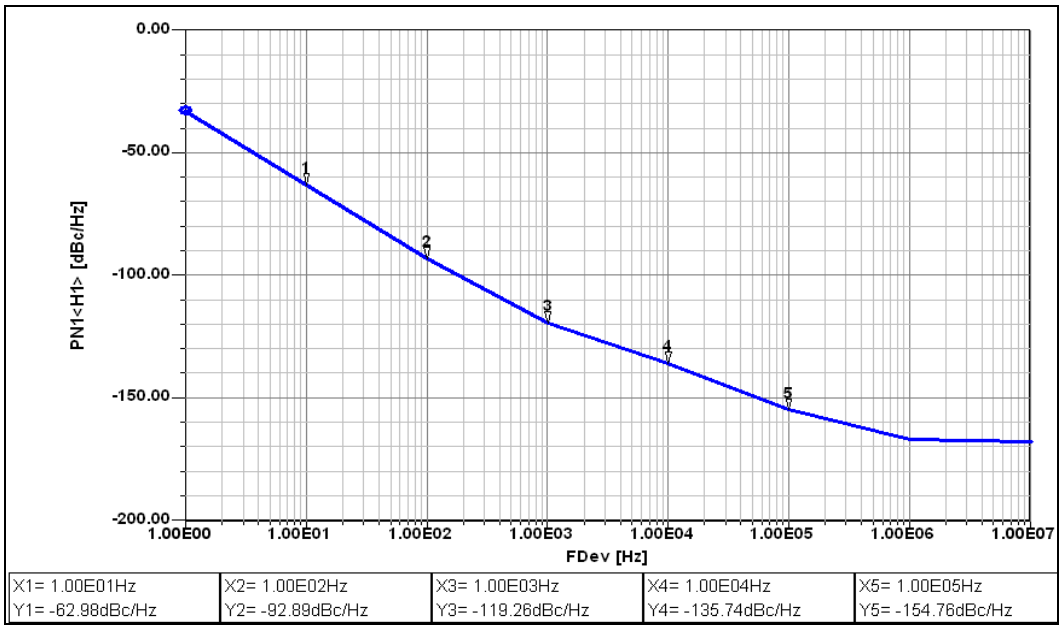


Figure 26: Phase noise of the 100MHz Butler oscillator.

The Pierce oscillator can also be modified as the Colpitts oscillator and the output power is extracted from the resonator while the crystal operates at series resonance. The collector of the transistor is not tuned to fundamental frequency of operation. Since the effective collector load must be capacitive, parallel resonance must be set lower than the frequency of operation. If the collector tank is tuned to a frequency between the fundamental and the overtone, the circuit will look inductive at the fundamental frequency and capacitive at the third overtone. Hence the circuit can operate only on the overtone. In this configuration the crystal filters the output signal and the oscillator transistor is operating in potentially lower noise configuration. The crystal current is lower than the circulating current in the loop, so the output is low. The low power into base stage may cause poor floor or high crystal power dissipation.

The capacitor C3 and inductor L3 forms the trap for fundamental frequency so that the oscillator can operate in the 3rd overtone mode. The nominal values are designed and capacitor C3 is made to be test on select so that proper oscillations are set. For our example C3 equal to 96pF was required to get the proper oscillations. The phase noise and the output power as a function of frequency is plotted in accompanying figures.

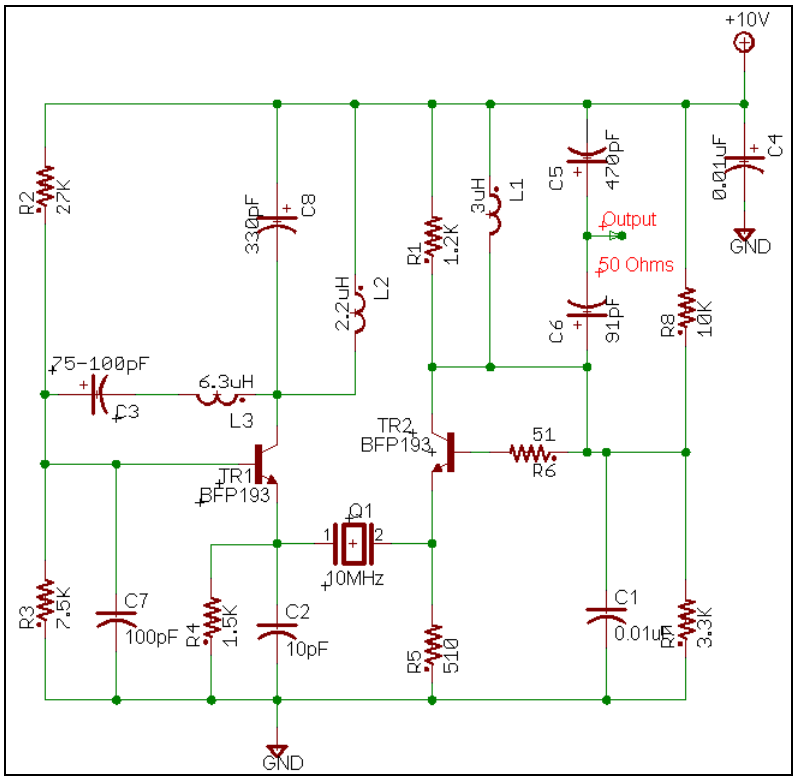


Figure 27: 10MHz 3rd overtone oscillator in Pierce Configuration

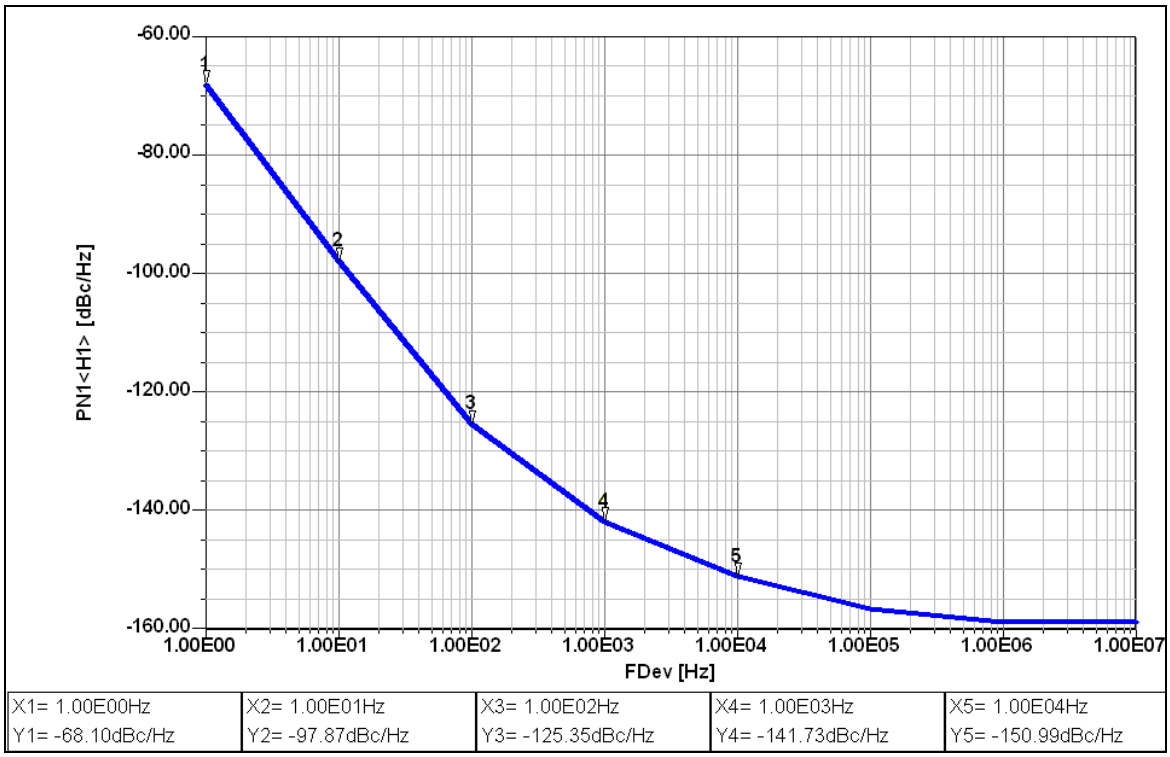


Figure 28: Phase noise response for 10MHz Pierce configuration oscillator.

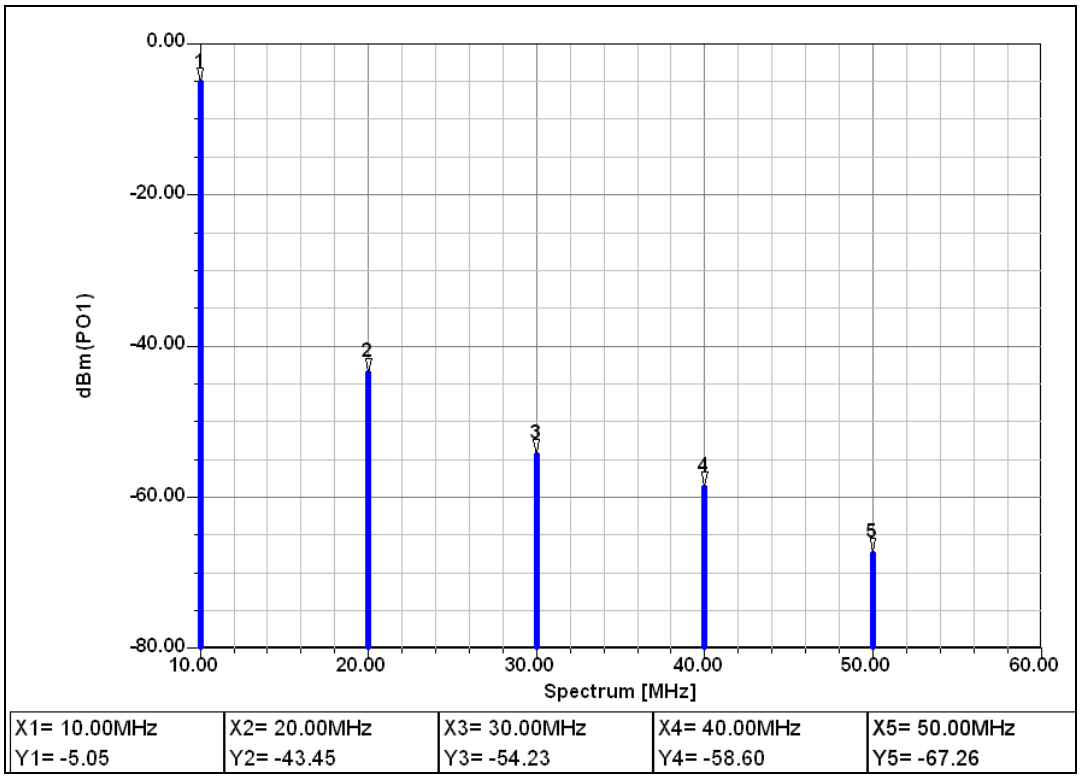


Figure 29: Output response for 10MHz Pierce configuration oscillator.

Limiting action: As we all know that the oscillator is an autonomous circuit. The noise signal in the active device or the transient from the power supply turn-on gets amplified, and continues to grow till it reaches the limiting action of the nonlinearities present in the circuit that provides the stable oscillations. This limiting action could be a result of the biasing done on the active device that controls the oscillating frequency or can be imposed from certain external means like Automatic Level Control (ALC).

The limiting action can be seen as the fundamental component of collector current, which is expressed as Fourier series, gets reduced by base-emitter voltage swing or by the collector-emitter voltage swing. The collector current, I_c, is expressed as a function of temperature and V_{be}, base-emitter voltage.

$$i_e(t) = I_s e^{\frac{qv_{be}(t)}{kT}}$$

$$v_{be}(t) = V_{BE} + v1\cos(\omega t)$$

$$i_e(t) = I_s e^{\frac{q(V_{BE}+v1\cos(\omega t))}{kT}} = I_s e^{\frac{qV_{BE}}{kT}} e^{\frac{qv1\cos(\omega t)}{kT}} = I_s e^{\frac{qV_{BE}}{kT}} e^{x\cos(\omega t)}$$

$$e^{x\cos(\omega t)} = \sum_n a_n(x)\cos(n\omega t) = I_0(x) + \sum_{n=1}^{\infty} I_n(x)\cos(n\omega t)$$

$$i_e(t) = I_s e^{\frac{qV_{BE}}{kT}}\left(I_0(x) + \sum_{n=1}^{\infty} I_n(x)\cos(n\omega t)\right) = I_s I_0(x) e^{\frac{qV_{BE}}{kT}}\left(1 + \sum_{n=1}^{\infty}\frac{I_n(x)}{I_0(x)}\cos(n\omega t)\right)$$

$$= I_{DC}\left(1 + 2\sum_{n=1}^{\infty}\frac{I_n(x)}{I_0(x)}\cos(n\omega t)\right)$$

where, I_{DC} is the dc emitter current, $I_n(x)$ is the modified Bessel function, I_s is the device saturation current, $v_{be}(t)$ is the drive voltage across base-emitter junction, V_{BE} is the dc base-emitter voltage and $v1\cos(\omega t)$ is the drive signal voltage. This exponential nature causes emitter current $i_e(t)$ to be composed of pulses the width of which decreases sharply as magnitude of $v_{be}(t)$ increases. For further understanding it is recommended to read the chapter 6 of reference 5.

The limiting action occurs due to the cut-off of the emitter current during part of the cycle because of the swinging of the base emitter junction below the contact potential. A colpitts oscillator design based on base-emitter voltage limiting is discussed below. The design values were computed using the algorithm presented by Benjamin Parzen. The load resistor obtained by this algorithm was 2.23KΩ and so a transformer was used to match with standard 50Ω load.

The schematic and the output phase noise simulated are shown in the adjoining figures. The design is more or less similar to the steps listed above except for the way the capacitance is computed here.

$$C1 = \frac{159000}{X1 * f}(pF)$$

$$X1 = \frac{v1}{I_1(x)}$$

$$Cb = C1 - \left(C_{bed} + C_{1M} + C_{bet}\right)(pF)$$

$$C_{1M} = C_{cb}\left(1 + \frac{V_L}{v1}\right)$$

$$C_{bed} = \frac{gm * 159000}{f_T}$$

$$Cn' = C_N - C_{cb}\left(1 + \frac{v1}{V_L}\right) - C_{ce}\ (pF)$$

$$C_N = \frac{159000}{XC_N * f}(pF)$$

$$XC_N = (1 - 0.2^2)\sqrt{\left(\eta R_{df} - \frac{R_{df}^2}{R_L}\right)R_L}$$

where, $X1$ is the drive dependent impedance, f is the operating frequency, C_{bet} is the total base-emitter capacitance, C_{cb} is the collector-base capacitance, V_L is the voltage across the load, R_{df} is the change in the resistance of resonator with slight variation in frequency, η is the power efficiency, gm is the large signal transconductance, f_T transition frequency of the transistor and R_L is the load resistor.

Based on the following equations a colpitts oscillator circuit was designed that uses the base-emitter limiting and the phase noise and output power was simulated.

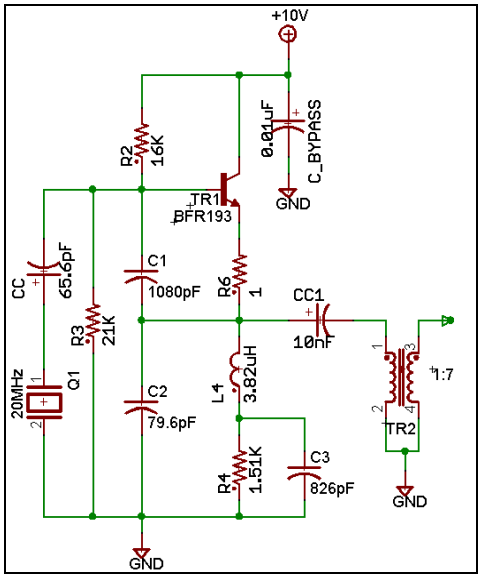


Figure 30: Colpitts schematic of 20MHz crystal oscillator implementing emitter-base limiting action.

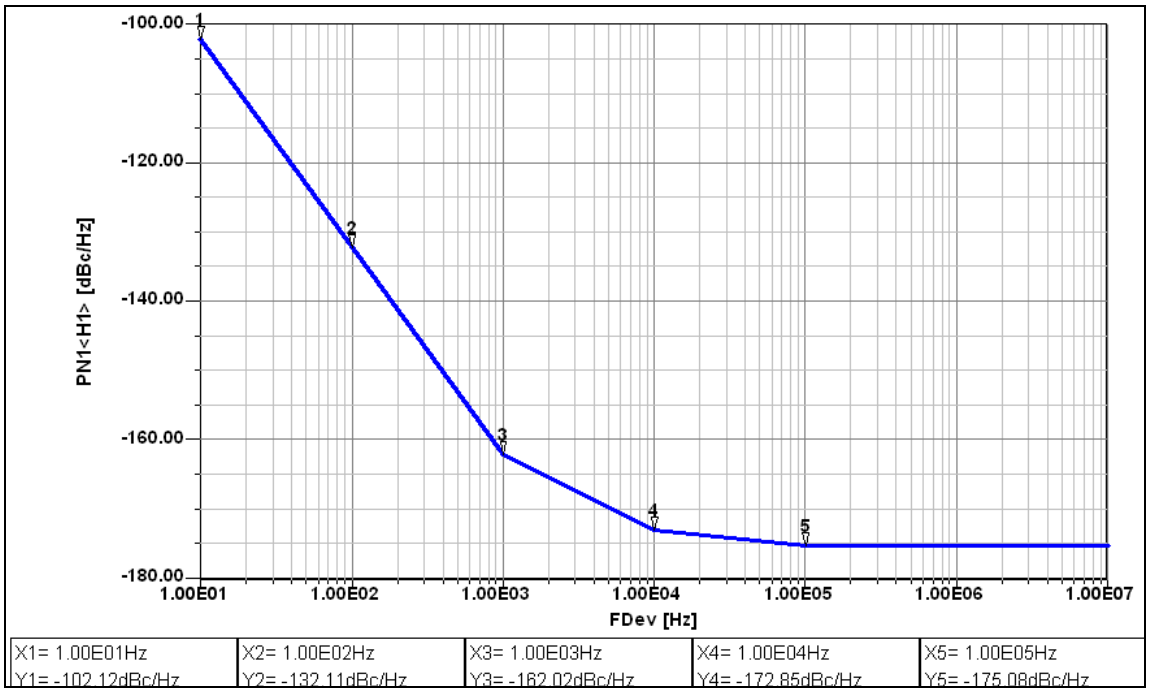


Figure 31: Phase noise response for 20MHz Colpitts-crystal oscillator implementing emitter-base limiting action.

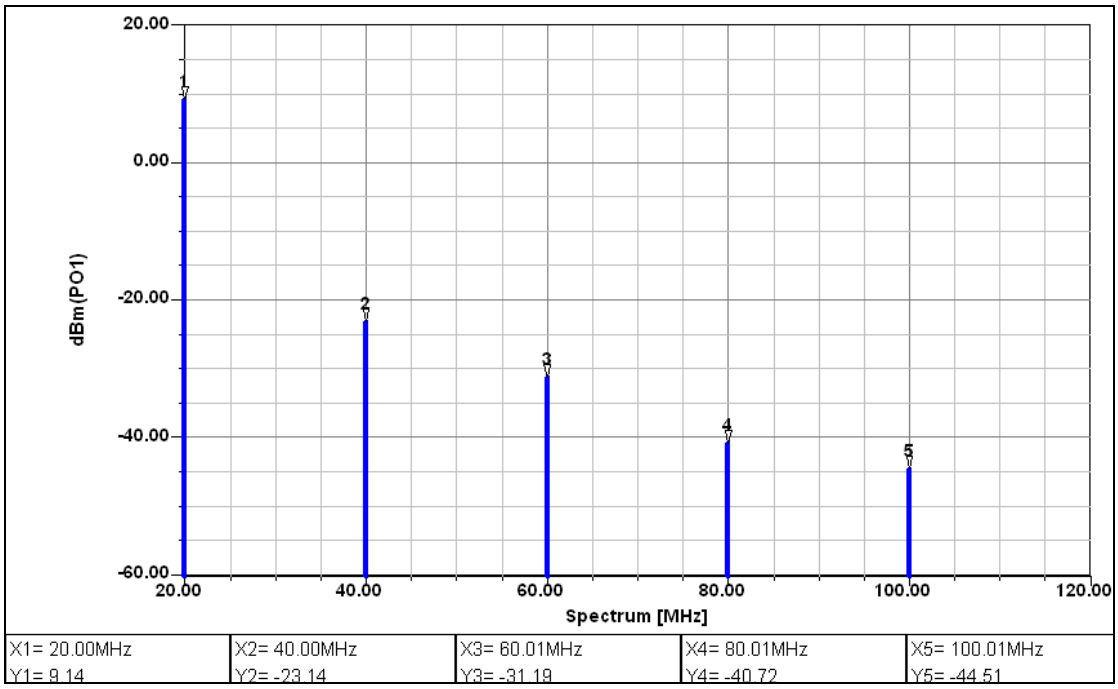


Figure 32: Simulated output response for 20MHz Colpitts-crystal oscillator implementing emitter-base limiting action.

Colpitts oscillator using the collector-base voltage limiting is discussed in short below. A major difference between the emitter-base limiting action over the collector-base limiting action is the overall power consumption. The supply current required is increased in collector-base limiting action due to greater loss in the resonator. Also the operational Q is lower in collector-base limiting action.

A circuit with collector-base voltage limiting action is implemented and shown in the figure 32. The design equations and algorithm can be referred from Ref. [8, chapter 6, 9].
The simulated phase noise and the output response are shown from the Ansoft serenade program.

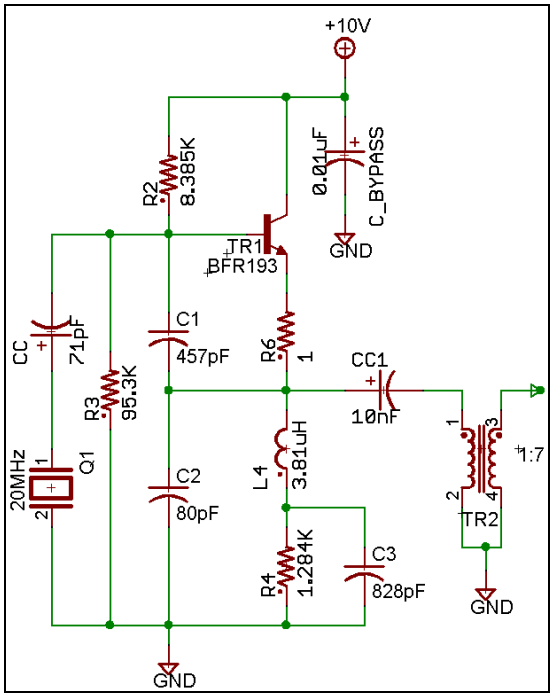


Figure 33: Colpitts schematic of 20MHz crystal oscillator implementing collector-base limiting action.

Few points of differentiation in the two limiting actions can be summarized as below. The base-emitter cutoff limiting is superior to collector-base limiting as long as the resistive impedance of the manufactured crystal is constant. As soon as the resistance change it will be difficult to have a production run of these designs. The change in the resonator impedance will have to be manually compensated. The emitter-base limiting has better supply sensitivity over collector-base designs. This is an advantage with the collector-base limiting action due less labor required. When the supply current is changed in base-emitter we can predict the direction of change and frequency changes can be compensated, while is collector-base limiting action the change of frequency will be difficult to predict. The base-emitter limiting action will give less degradation to the operating Q of the circuit, and provide higher frequency operation due to larger collector-emitter voltage. For lower drive level voltage to operate the

crystal, the base-emitter limiting action should be used as it becomes more difficult to maintain all the biasing voltage constant.

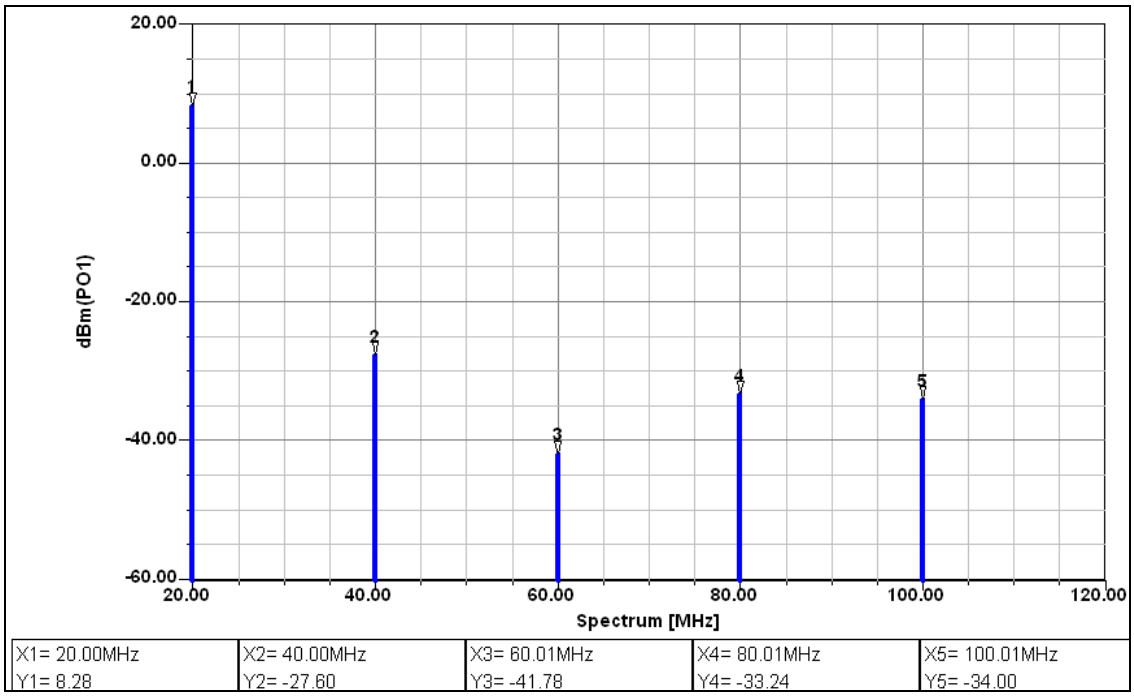


Figure 34: Phase noise response for 20MHz Colpitts-crystal oscillator implementing collector-base limiting action.

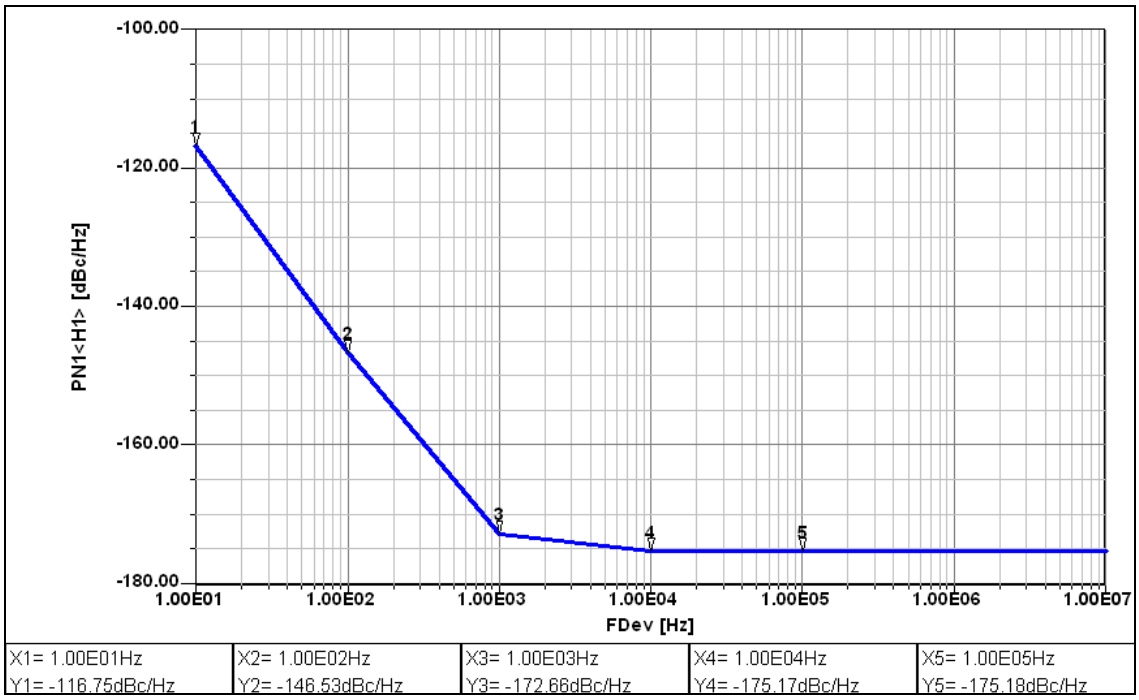


Figure 35: Simulated output response for 20MHz Colpitts-crystal oscillator implementing collector-base limiting action.

Another example of butler oscillator is the following circuit from [8]. The algorithm from Parzen was used to compute the required values of components (not standard components).

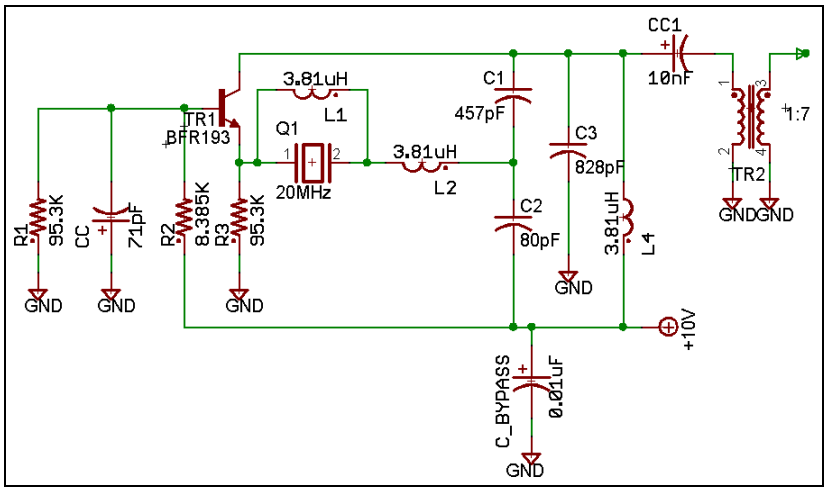


Figure 36: 20MHz Butler-crystal oscillator.

The circuit of 20MHz butler oscillator was simulated in CAD software and the simulated response of phase noise and output power are as shown in the adjoining figure. The transformer was used at the output to match the impedance to 50 ohm.

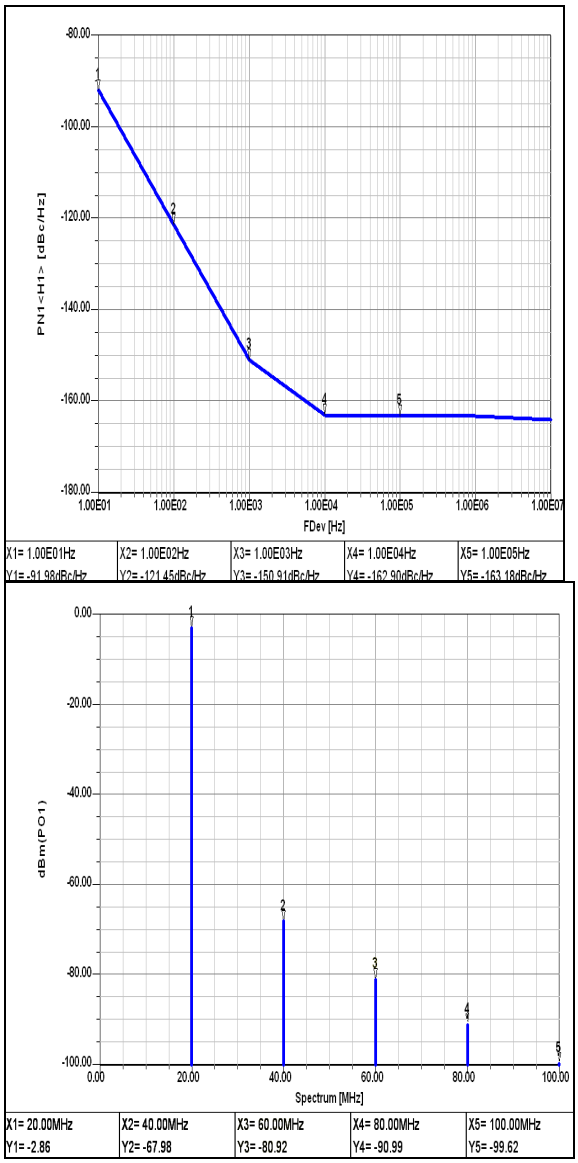


Figure 37: a) Simulated phase noise of 20MHz Butler oscillator and, b) simulated output response

Few more examples studied are presented here from reference 21.

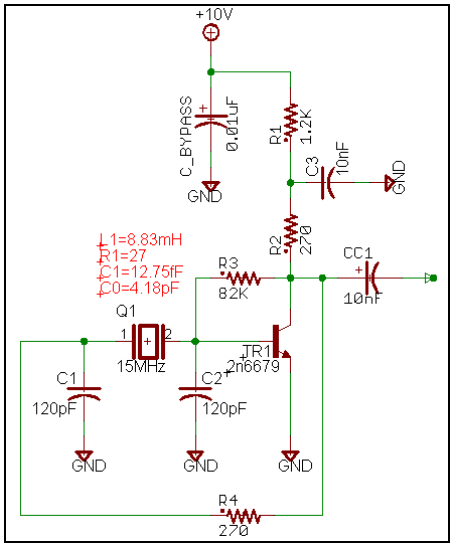


Figure 38: 15MHz Pierce Oscillator.

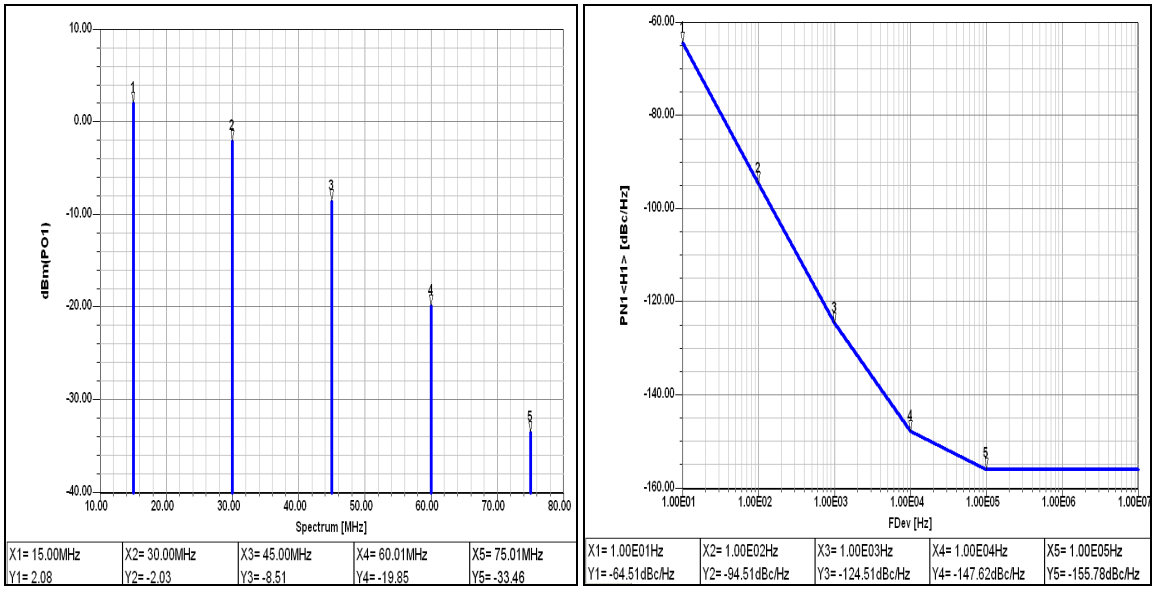


Figure 39: 15MHz Pierce Oscillator (a) Output Response, (b) Phase noise

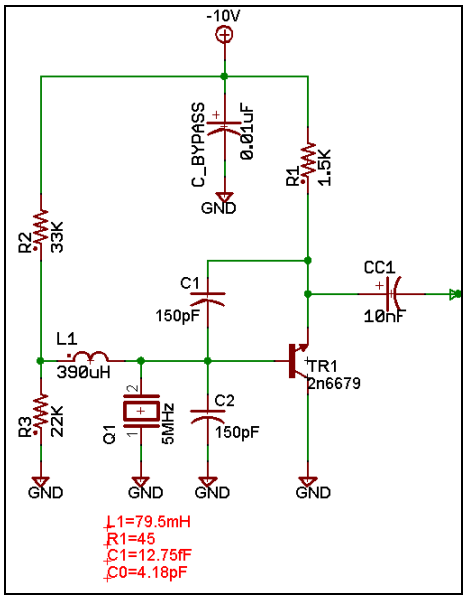
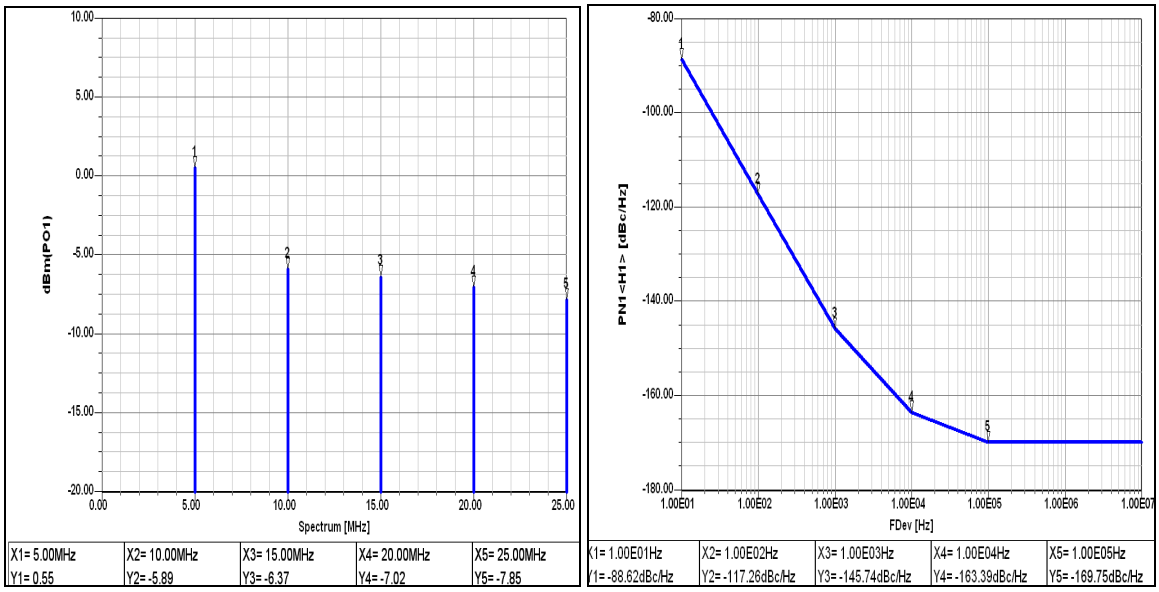


Figure 40: 5MHz Colpitts oscillator.



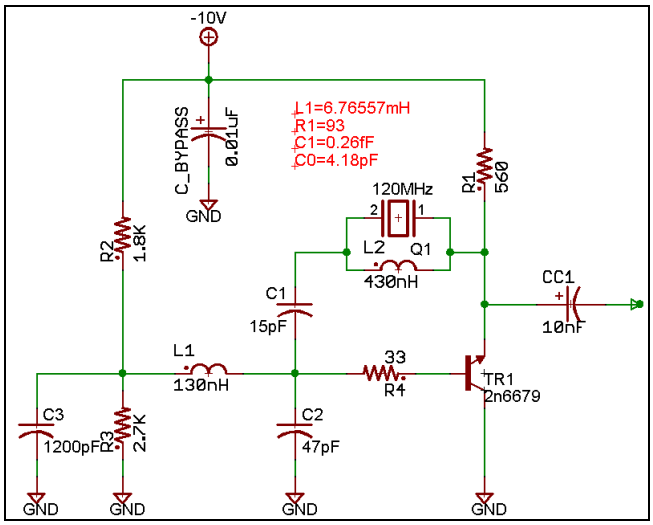
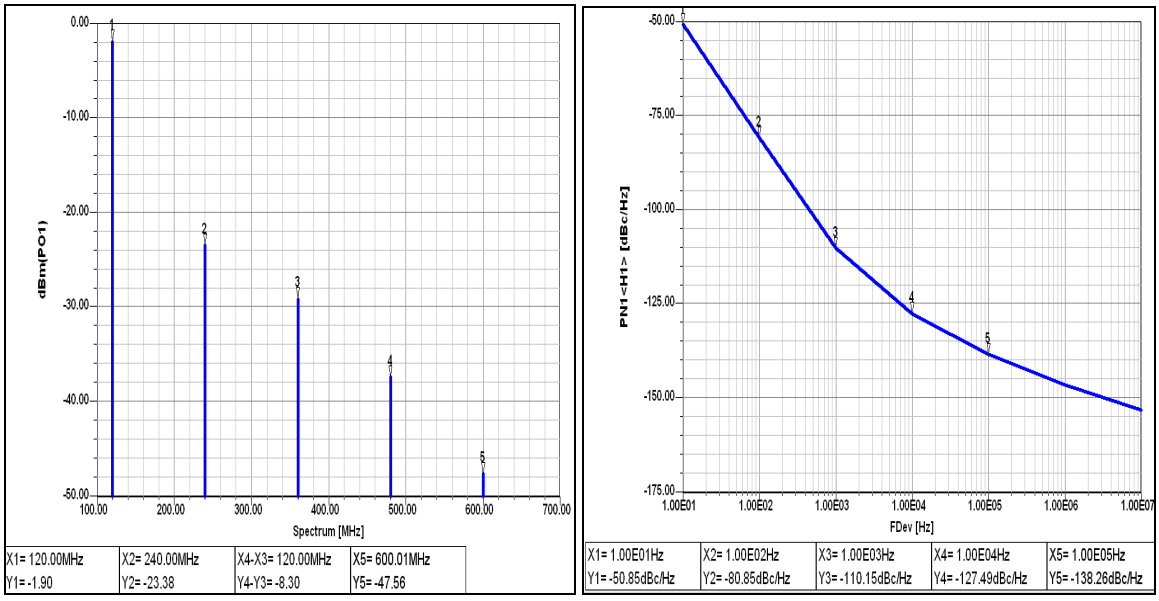


Figure 42: 120MHz Butler oscillator (Emitter output).



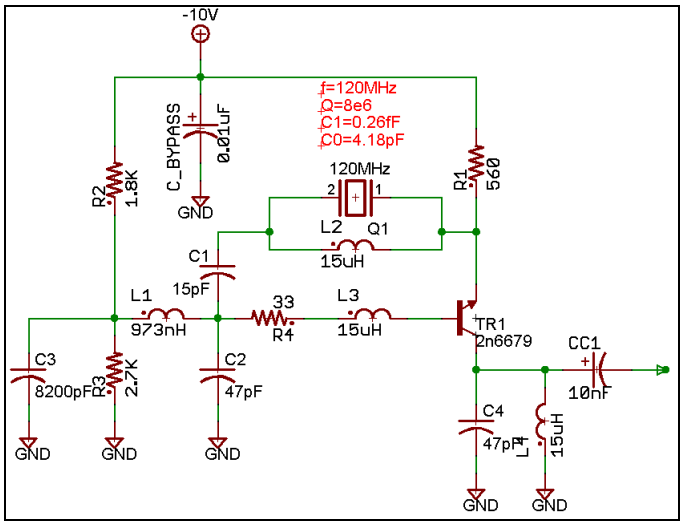
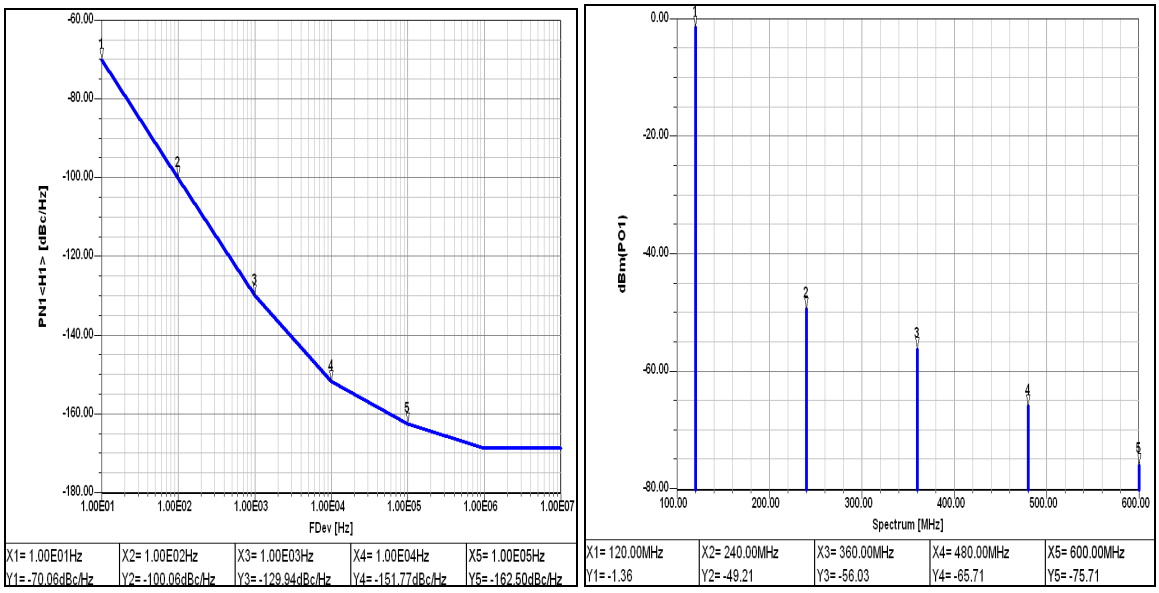


Figure 44: 120MHz Butler oscillator output at the collector.



This section should be used only as guideline aids to selecting the configuration type for the oscillator once the design specifications are decided. Crystal oscillators above 100MHz can be easily built, but it is often preferable to use a lower frequency oscillator followed by the frequency multiplier. This arrangement is often more practical in production environment. There are many different types of oscillators apart from the ones listed here that offer excellent performance in certain areas. These guidelines are for few commonly used simple to design configurations that still offers good performance. The principal difference between the Pierce and Colpitts configuration is the choice of signal ground. One must note that since the only change is the choice of signal ground, the negative resistance equation that governs the Colpitts oscillator are also valid for small signals will also be valid for Pierce oscillator. This means that the small signal gain requirements are the same and the circuit will oscillate if, $gmXc_1Xc_2 \rangle R_E$, where R_E is the real part of the series impedance across the crystal, Xc_1Xc_2 are the impedance of the capacitance in the voltage divider and gm is the transconductance for the transistor. Even though this is true still the performance for both of them will be quite different due to different limiting action, occurring under the large signal conditions. All these configurations can be optimized to get more-or less the same phase noise at the cost of certain parameters. Note: Overtone crystals are not a good choice when large frequency deviation is required. The pullability of crystals (change in frequency) is inversely proportional to the square of the overtone number, so as the higher overtone crystals are used the pullability available reduces.

$$\frac{C_N}{N^2} = \frac{2*\Delta f\left(C_0 - C_L\right)}{f*10^6} \Rightarrow \frac{1}{N^2} \propto \Delta f$$

Summarizing the general advantages and disadvantages of the various configurations of oscillator:

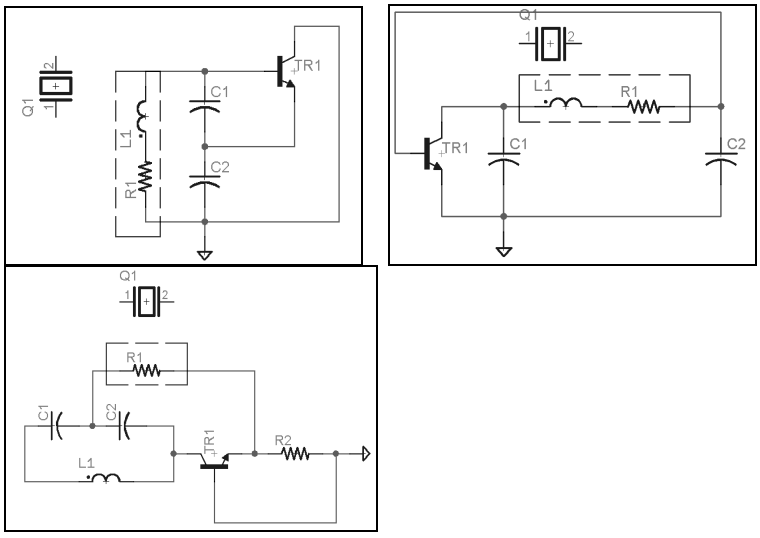


Figure 46a: Colpitts Configuration Figure 46b: Pierce Configuration Figure 46c: Butler Configuration

Colpitts oscillator:
This configuration is designed to take the output from the emitter and the collector is tied directly to the supply voltage. This design is fairly simple and the performance is moderate to good. As there is no collector resistor, the limiting is due to the cutoff in transistor. With crystal, this design can be used for very small frequencies and needs modifications in it as the frequency increases. The Colpitts configuration works very well for low aging and good performance oscillators upto 50 MHz. The amplifier in Colpitts is an emitter-follower. Feedback is provided via a tapped capacitor voltage divider (C1 and C2). The cost to build these oscillators is less and so is the number of components used in the circuit, typically less than ten components will be used.

Semi-isolated Colpitts oscillator (Output from Collector):
This configuration is designed to take the output from the collector. More power is available at the output from collector than the power extracted from the resonator. The miller capacitance limits the operation of these configurations at high frequencies. But the advantage of such a configuration is the impedance in the collector branch can be tuned to its higher harmonics. This means for high frequency applications a frequency multiplication action from such configuration should be used with the collector tank tuned to its higher harmonic. The isolation from load to the oscillator circuit is also much better when the output is a harmonic of the oscillator frequency. The Coupling capacitor loads the circuit and more power is extracted. But capacitive load will reduce the operating Q of the circuit and the transistor may go into saturation if the load is too high.

Semi-isolated Configuration (Cascode Configuration, Output from Collector):
The output of the semi-isolated colpitts configuration can be dc coupled into a common base amplifier in a cascode arrangement. This modification gives excellent isolation to the load and allows for a much larger collector load in the second transistor. These circuits are slightly more complex to design and manufacture. Also we need a higher power supply requirements to properly bias the amplifier and thus have more power consumption. This kind of design is more preferred at the higher frequency range than the traditional Colpitts. As the common base amplifier is used in this configuration the degradation of Q, caused by the low impedance of emitter terminal of transistor, will be less. The crystal is placed such that there is current flow through the resonator that makes the crystal to act as a filter there by providing a better noise-floor.

Driscoll oscillator:
Driscoll is a more complex crystal oscillator with excellent performance characteristics. It is a cascaded stage of inverting common emitter amplifier along with the phase shifter. Without the crystal, this circuit is more effectively like a Pierce oscillator or the old Vackar VFO. The Driscoll oscillator basically turns the semi-isolated cascode configuration around and uses the common emitter (CE) oscillator with the crystal connected between the emitter and ground. This results

in degradation of Q of the crystal, which makes contact with the collector terminal of the transistor that has low impedance due to the input stage of CE amplifier.

Semi-isolated Colpitts oscillator (Output from Collector):
Another modified version of semi-isolated Colpitts oscillator is one in which the output is extracted from the resonator. The principal disadvantage of this circuit is low power at the output. These circuits are terminated by a cascode stage at the output. By extracting the resonator power through crystal, the crystal acts as a very narrowband filter on noise generated by the oscillator stage. The common base stage offers a very low impedance and the Q degradation will be very small. The ratio of crystal power to oscillator output power is equal to ratio of crystal resistance to common base input. As the output is from the resonator itself the harmonic contents are suppressed more in this configuration.

Pierce configuration:
The Pierce oscillator is capable for a good performance at high frequencies. Note that if the emitter is grounded for the Colpitts, the configuration changes to Pierce. The important difference of biasing arrangement in Pierce oscillator increases the effective resistance of the crystal thus reducing its Q and decreasing the loop gain. The impedance at the collector may cause transistor saturation. If optimized for low aging then the crystal power may also become excessive. There is some tendency of spurs at high frequency. The package inductance at the base pin of the transistor will generate the undesired resonance at very high frequency. For example in 10MHz oscillator a response may also be present at 5GHz.

Modified Pierce Configuration (Output from resonator):
In the modified Pierce oscillator configuration the crystal operates in a series resonant mode, so we can tune out the crystal motional capacitance of the crystal giving more linearity and reducing the out-of-band noise. In series mode the current in the crystal will be much less than the available power of the oscillator. This generates the need for a buffer amplifier at the output to achieve the power requirement. Both these parameters, less current at the output and the buffer amplifier increase the far-out phase noise. But the crystal acts as a filter itself for the close-in noise.

Butler configuration:
The Butler oscillator gives good performance for frequencies from 10MHz to VHF. This is because the collector to base capacitor is effectively grounded. Butler oscillators are quite susceptible to spurious resonances. The amplifier is an emitter follower. The output of the common butler oscillator is taken from the ac grounded base of the oscillator. When a high frequency operation is desired the tank circuit is used in collector, which is used as the output terminal. To operate on the overtone frequency the tank circuit resonance is tune changed. The advantage of the butler oscillator is that a small voltage exists across the crystal, reducing the stress on the crystal.

Some Validated Circuit:
(Left Blank Intentionally as Separator)

Schematic from figure 18 was built and validated for truth. The overall built circuit was as follows.

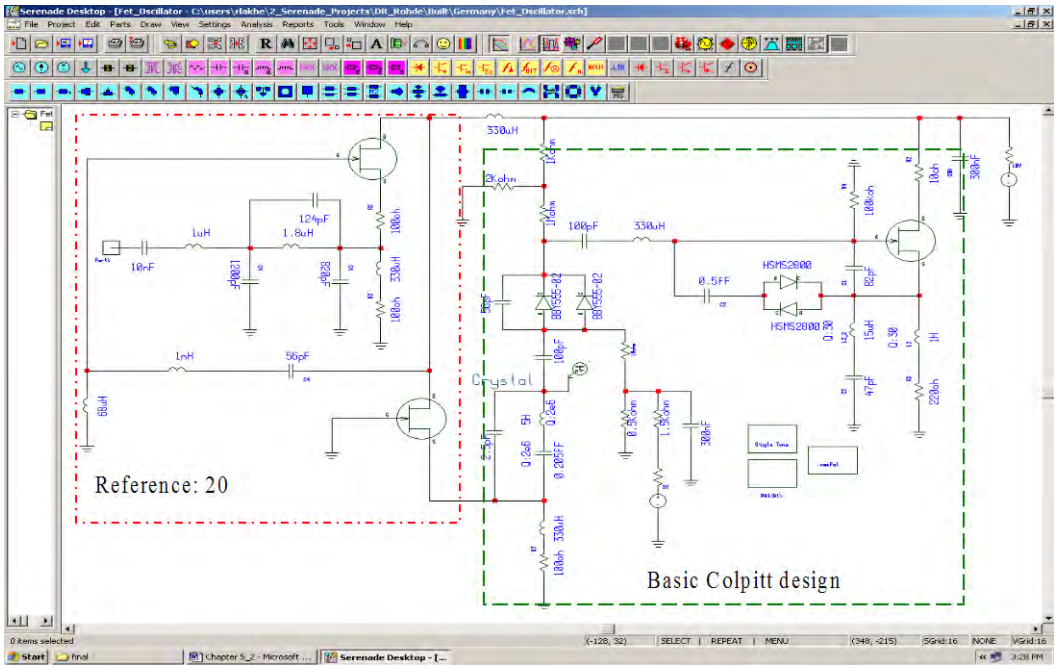


Figure 47: 5MHz Colpitts oscillator with output from resonator.

In the normal Colpitts oscillator the output is taken from the resonator, reference 20 and then passed through an amplifier and filter. When the output is taken from the resonator the output is less compared to the output we can get from collector/ drain or the emitter/source of the active device. Hence we need an amplifier at the output stage, but this results in slightly high harmonic content, so a filter is used to suppress it. The simulated response for the overall circuit is as shown below in figure 48. Figure 49 shows the measured response of the circuit.

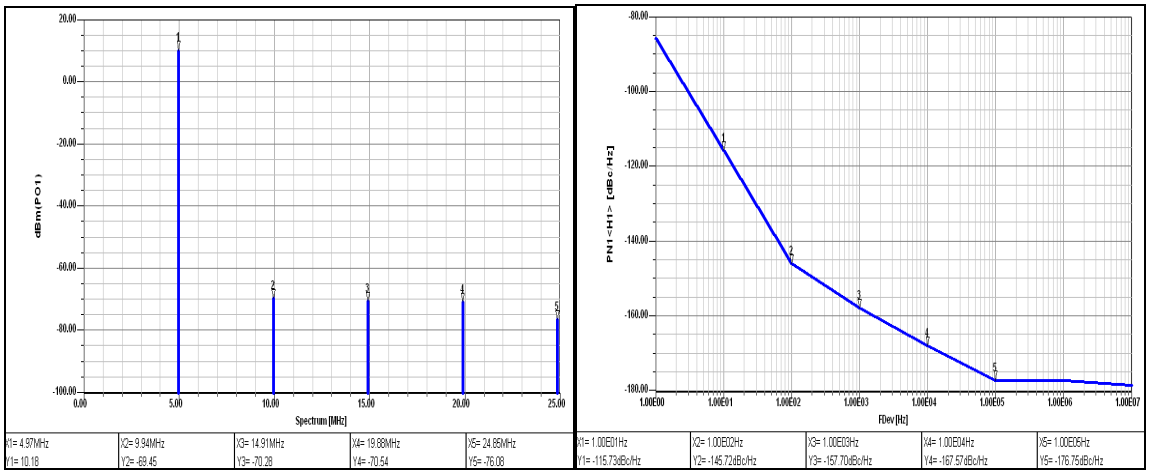


Figure 48: (a) 5MHz Colpitts oscillator output with harmonic suppression around –80dBc/Hz (b) Phase noise of the 5MHz Colpitts oscillator.

To validate the design approach, a commercial 155.6 MHz VCXO was used as an example to apply the concept of mode-feedback, and mode-coupling mechanism. The promising alternative for high performance VCXO at 155.6 MHz is overtone mode, which is similar in concept to a harmonic, with the exception that crystal oscillation overtones are not exact integer multiples of the fundamental. The new approach includes dynamic noise filtering, mode-feedback, noise-feedback, and mode coupling for optimum group delay to enhance the loaded Q and suppress mode-jumping phenomena (especially when the crystal resonates at higher odd-order overtone modes).

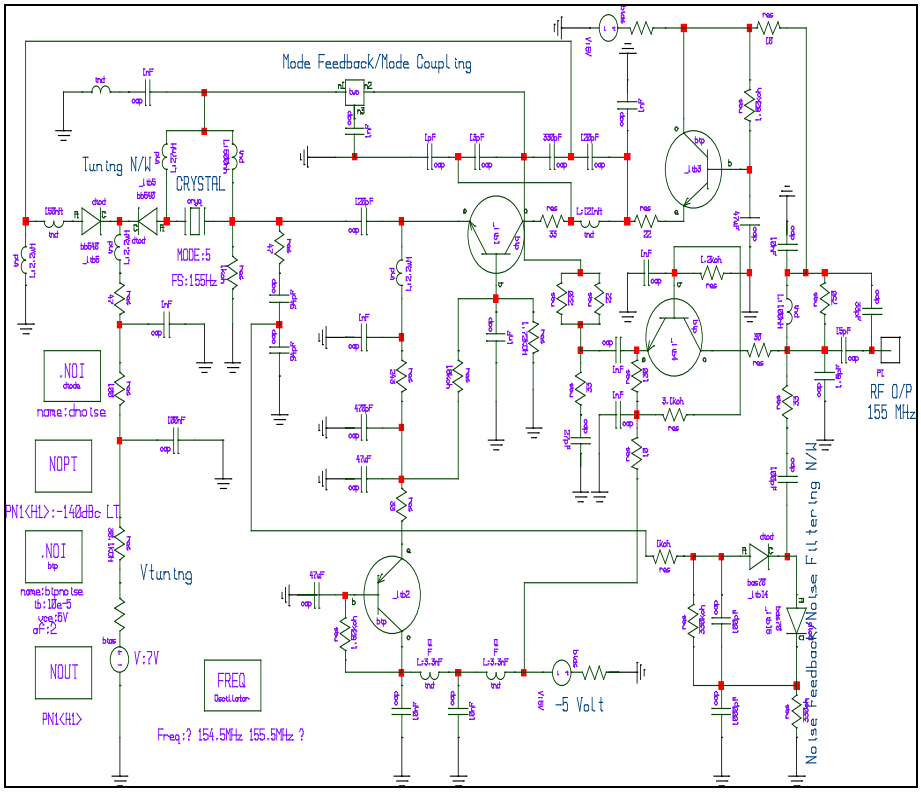


Figure 50: 155.6 MHz Mode-Feedback 5th overtone VCXO (Patent Pending)

Figure (50) shows the 5th overtone 155 MHz VCXO circuits in which higher order mode is coupled through output path and feedback to the point where resonator impedance shows steep change of phases, thereby, maximization of group delay [12]-[19]. Additional improvement in the phase noise is achieved by dynamically optimizing noise-feedback and mode-coupling mechanism. The dynamic noise-feedback is an effective method to reduce the 1/*f* noise. By introducing an additional low frequency negative feedback loop, the close-in noise is reduced by approximately 10-15 dB in the flicker region. A mode-feedback and noise filtering offers significant improvement in phase noise performances (-139

dBc/Hz @ 100Hz offset for 155.6 MHz carrier frequency) and was validated using cad software.

Figure (51) shows the measured phase noise plot, which closely agree with the simulated result for both approaches (with and without mode-feedback). At lower offset (1Hz), improvement in phase noise performance is limited due to the influence 1/*f* noise, which can be optimized by selecting transistor that has low value of 1/*f* noise.

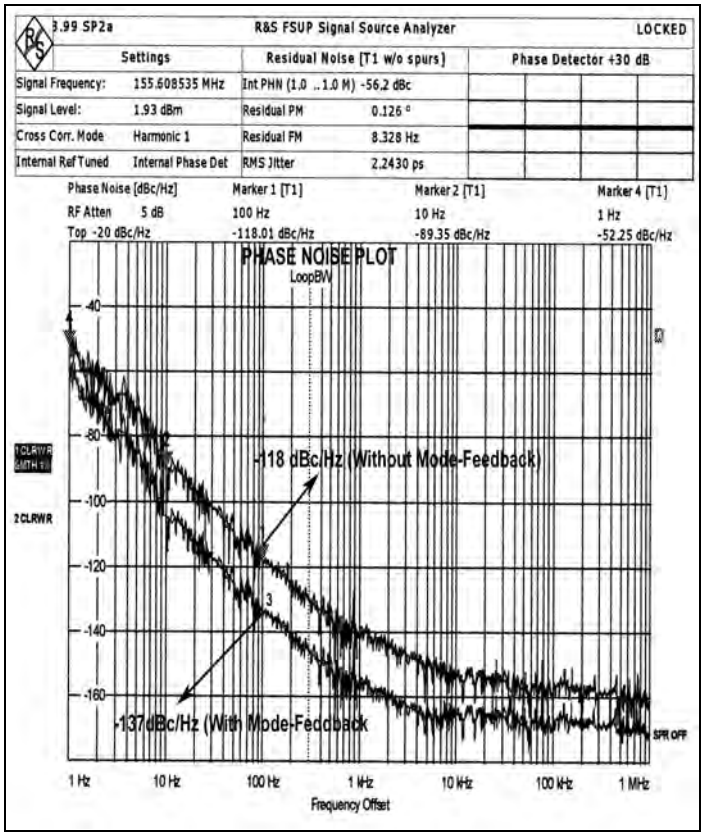


Figure 51: Measured phase noise plots for 155.6 MHz 5th overtone VCXOs

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Some Thoughts on Designing Very High Performance VHF Oscillators

Building a very high performance oscillator requires some careful engineering design work.

A *QEX* article by Colin Horrabin about part of the HF7070 receiver retriggered my interest in VHF oscillators / VCOs. (The Development of the Low Phase Noise Double Tank Oscillator, Colin Horrabin, G3SBI, *QEX* Nov/Dec 2014.)[1] He claimed that a type of push-pull oscillator would improve the phase noise roll-off from 20 dB/dec to 40 dB/dec, and he also referred to some receiver measurements made by Rob Sherwood. The data points I reviewed do not support this theory, and the reciprocal mixing tests are not conclusive, because two signal generators were used. The correct comment is that the type 2, high-order phase locked loop inherently has a 40 dB/dec roll off, not the oscillator.

The single resonator oscillator using lumped elements by itself is a good solution. The slope of the radiation resistance of a quarter wave resonator does not change if a half wave resonator will be chosen, so a push-pull oscillator is not better.

The symmetrical oscillator proposed by Horrabin just uses twice the inductance, and the two capacitors, now in series, have half their individual value. In simple terms, Horrabin changed the LC ratio, which cannot have any influence on the phase noise nor the slope. The loading from the transistor may now be different.

The best way to get the phase noise evaluation right is to use a dedicated phase noise system like the Rohde & Schwarz FSUP 26 phase noise tester, spectrum and signal analyzer that the ARRL Lab has to make their measurements. At the same time, it is useful to calculate the best possible phase noise based on physics and using a low flicker noise FET. FETs in oscillators are limited to about 500 MHz because of their cut-off frequency. For higher frequencies SiGe HBT (heterojunction bipolar transistors) are superior, and because modern communications equipment uses PLL systems with sufficiently wide bandwidth, the flicker corner frequency inside the loop bandwidth is of less concern. Outside the loop bandwidth the loaded *Q* of the resonator determines the phase noise. If Colin Horrabin's paper is correct, the roll off has to be 20 dB/decade or 40 dB/decade but not 30 dB/decade, which would be due to flicker noise. A VCO with 1 kHz loop bandwidth was quoted. I will comment on this later.

Only for oscillators using the evanescent mode and distributed elements, like (multiple) coupled lines, the configuration results in an increased operating *Q*, which for lumped circuit components is not possible. Using coupled transmission line structures (distributed components) is a better choice. At VHF, this is prohibitive because of size.

An evanescent wave is a near-field wave with an intensity that exhibits exponential decay without absorption as a function of the distance from the boundary at which the wave was formed. Evanescent waves are solutions of wave equations, and can in principle occur in any context to which a wave equation applies. They are formed at the boundary between two media with different wave motion properties, and are most intense within one third of a wavelength from the surface of formation.

As evidence of how moving from lumped to distributed techniques can improve oscillator performance at frequencies where *LC* tank circuits become problematic, Figure 1 compares the difference in phase-noise performance obtainable using a resonator consisting of an ideal 2 nH inductor and a ¼ λ transmission line (11 Ω, 90° long at 2.6 GHz, attenuation 0.1 dB/meter) with the transistor biased by constant-current and constant-voltage sources for a simulated BJT Colpitts oscillator operating at 2.3 GHz. This is a result of the magnetic coupling, which does not exist for lumped (discrete) inductors.[2] The articles described in Notes 3, 4, 5, and 6 address this topic in practical applications.[3, 4, 5, 6]

The 1 kHz loop bandwidth would be dangerous because mechanically introduced microphonics would then not be suppressed. A 10 kHz loop bandwidth is much more opportune. Better synthesized local oscillators (LOs) use multiple loops and direct digital synthesis (DDS) systems, which allow such wide loop bandwidth. Many modern receivers and transceivers apply this technique.[7, 8] Even better today, software defined radios (SDR) can have excellent phase noise performance. (See the R&S EB-500 9 kHz to 6 GHz receiver: **http://n1ul.com/eb500.htm**.)

[1]Notes appear on page 40

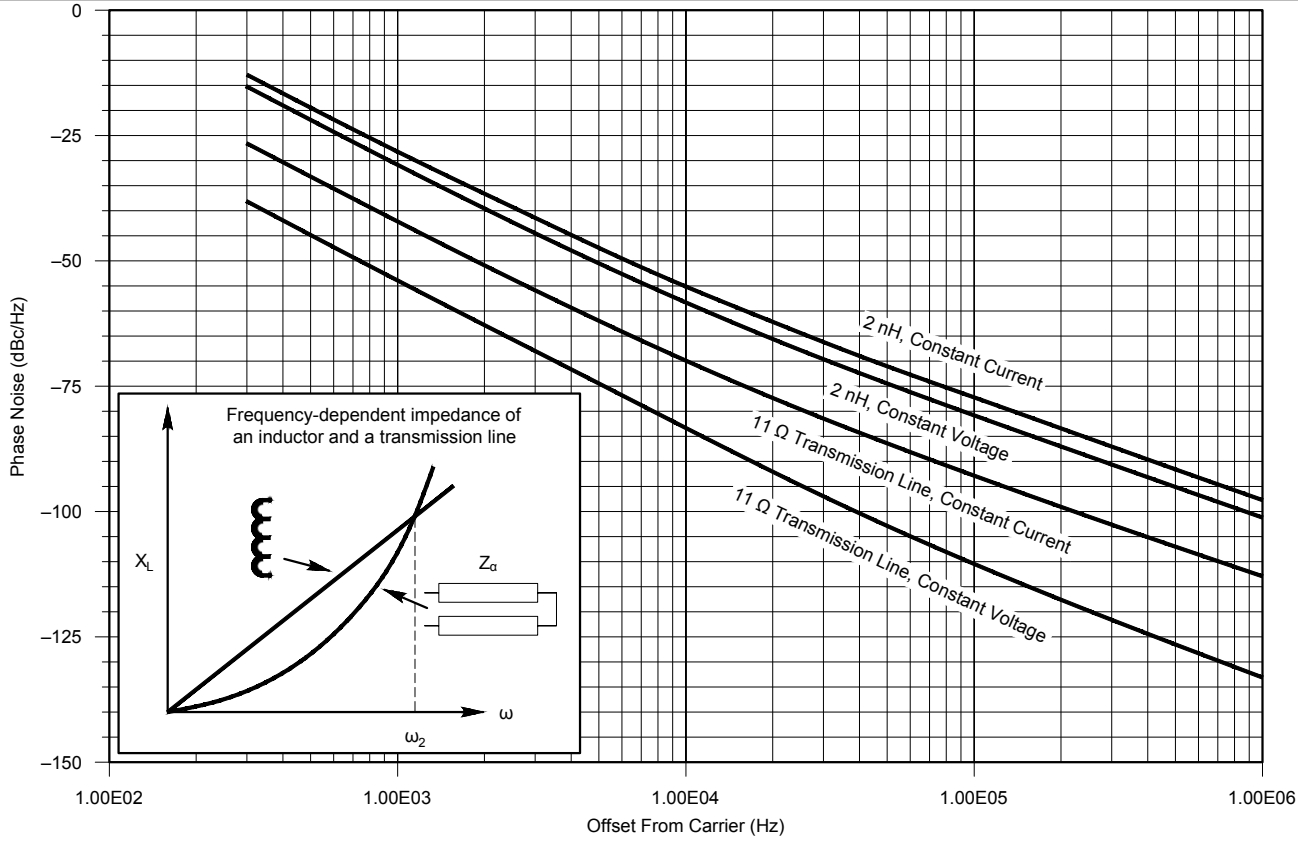
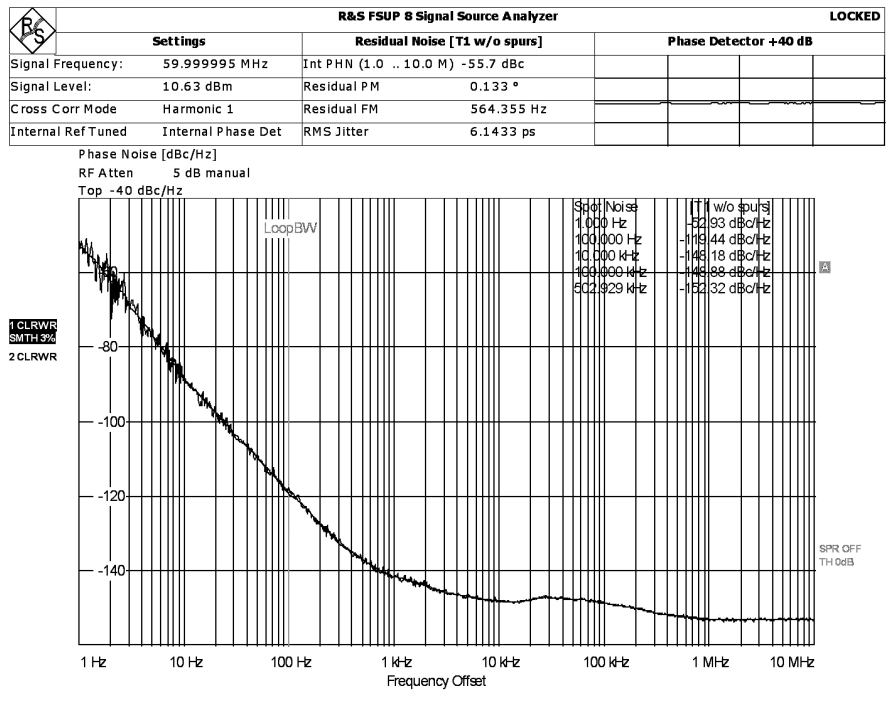


Figure 1 — This graph shows the phase-noise performance of a 2.3 GHz BJT oscillator with a resonator consisting of an inductor (2 nH) and a ¼ λ transmission line (11 Ω, approximating the behavior of a dielectric resonator) with bias from a constant-current source and a low-impedance, resistive constant-voltage source.

Figure 2 — This screen shot from the Rohde & Schwarz FSUP signal source analyzer shows the measured phase noise of a synthesized 60 MHz LO. The –150 dBc/Hz limit is a result of the buffer amplifier. It requires a special design to obtain better values. Even at +10 dBm output there is a practical limit of about –175 dBc/Hz for a VCO and buffer. Some additional useful information can be found in the articles of Notes 9 and 10.



Transceivers with a first IF between 45 to75 MHz, require such VHF oscillators. This paper will try to demystify this topic and will show the correct mathematics, proven schematics and measured data. It is partly based on *RF/Microwave Circuit Design for Wireless Applications* (see Note 2). Figure 2 shows the measured phase noise performance of a modern receiver that uses a 60 MHz LO. This measurement was made using the aforementioned R&S FSUP signal analyzer.

Some Equations

David Leeson was the first to help us understand the mechanics of phase noise, based on a low pass filter approach in 1966.[11] Dieter Scherer and others improved the model further.[9, 10, 12, 13, 14]

Phase noise is defined in terms of the noise spectral density, in units of decibels below the carrier per hertz, and is based on Equation 1 by Leeson, Scherer and Rohde.

$$\pounds(f_m) = 10\log\left[\frac{P_{sideband}(f_0+f_m,\ 1\ Hz)}{P_{carrier}}\right] = 10\log\left[S_\varphi(f)\right] \qquad \text{[Eq 1]}$$

$$\pounds(f_m) = 10\log\left\{\left[1+\frac{f_0^2}{(2f_mQ_L)^2\left(1-\frac{Q_L}{Q_0}\right)^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_0}+\frac{2kTRK_0^2}{f_m^2}\right\} \qquad \text{[Eq 1A]}$$

where:
$\pounds(f_m)$ is the ratio of the sideband power in a 1Hz bandwidth at f_m to total power in dB
f_m is the offset frequency from the carrier
f_0 is the carrier frequency
f_c is the flicker corner frequency
Q_L is the loaded Q of the tuned circuit
Q_0 is the unloaded Q of the tuned circuit
F is the noise factor
k is Boltzmann's constant
T is the temperature in Kelvins
P_0 is the average power at oscillator output
R is the equivalent noise resistance of the tuning diode
K_0 is the oscillator voltage gain.

When adding an isolating amplifier, the noise of an LC oscillator is determined by Equation 2.

$$\pounds(f_m) = 0.5\times10\log\left[\left(S_\varphi(f_m)\right)\right]$$

$$\pounds(f_m) = 0.5\times10\log\left\{\frac{\left[a_RF_0^4+a_E\left(\frac{F_0}{2Q_L}\right)^2\right]}{f_m^3}+\frac{\left[\left(\frac{2GFkT}{P_0}\right)\left(\frac{F_0}{2Q_L}\right)^2\right]}{f_m^2}+\left(\frac{2a_RQ_LF_0^3}{f_m^2}\right)+\frac{a_E}{f_m}+\frac{2GFkT}{P_0}\right\} \qquad \text{[Eq 2]}$$

where,
G = compressed power gain of the loop amplifier
F = noise factor of the loop amplifier
k = Boltzmann's constant
T = temperature in kelvins
P_0 = carrier power level (in watts) at the output of the loop amplifier
F_0 = carrier frequency in Hz

f_m = carrier offset frequency in Hz

$Q_L (= \pi F_0\tau_g)$ = loaded Q of the resonator in the feedback loop

a_R *and* a_E = flicker noise constants for the resonator and loop amplifier, respectively.

The problem with this design equation, which everyone likes to quote, is that it works after the fact. That means the designer does not know the output power, the flicker corner frequency, and the large signal noise figure, and finally, because the right part of the equation is the noise from the tuning diode, the value of the equivalent noise resistor, *R*!

Influence of the Tuning Diode

It is possible to define an equivalent noise resistor, R_{aeq}, which when inserted into Nyquist's equation, determines an open-circuit noise voltage across the tuning diode.

$$V_n = \sqrt{4kT_0R\Delta f} \qquad \text{[Eq 3]}$$

where:
$kT_o = 4.2\times10^{-21}$ at about 300 K
R is the equivalent noise resistor
Δf is the bandwidth.

Practical values of R_{aeq} for carefully selected tuning diodes are in the vicinity of 200 Ω to 50 kΩ. We can now determine the noise voltage, V_n.

$$V_n = \sqrt{4\times4.2\times10^{-21}\times10{,}000} = 1.296\times10^{-8}V\sqrt{Hz}$$

This noise voltage generated from the tuning diode is now multiplied with the VCO gain, K_o, resulting in the RMS frequency deviation.

$$(\Delta f_{rms}) = K_0\times\left(1.296\times10^{-8}V\right)\text{in 1 Hz bandwidth} \qquad \text{[Eq 4]}$$

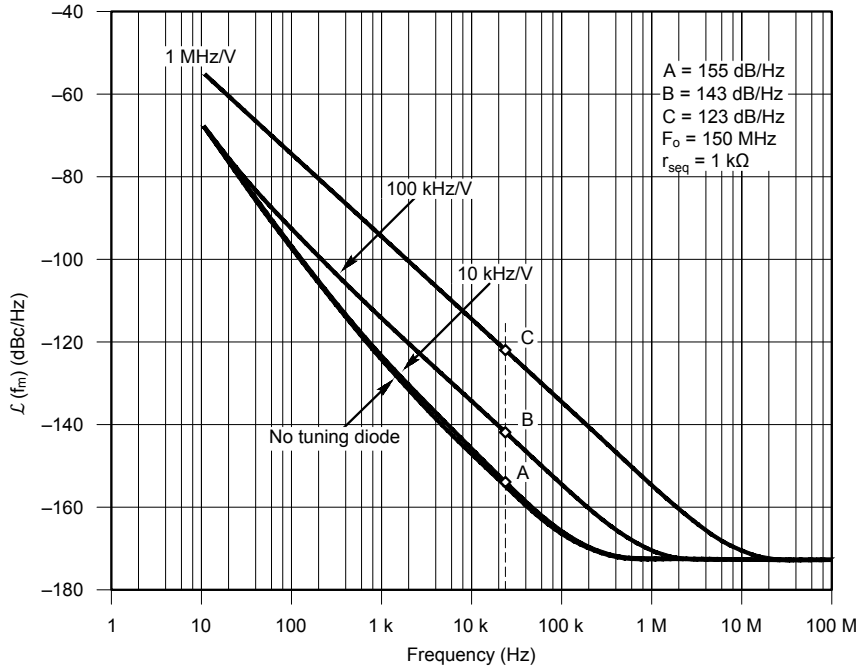


Figure 3 — This graph shows the influence of the diode noise of a VCO at 150 MHz.

To translate this into an equivalent peak phase deviation, we will use Equation 5.

$$\theta_d = \frac{K_0\sqrt{2}}{f_m} \times \left(1.296 \times 10^{-8}\right) \text{rad in 1 Hz bandwidth} \qquad \text{[Eq 5]}$$

Or, for a typical oscillator gain of 100 kHz / V:

$$\theta_d = \frac{0.00183}{f_m} \text{rad in 1 Hz bandwidth} \qquad \text{[Eq 6]}$$

For f_m = 2.4 kHz (typical spacing for adjacent-channel measurements for good SSB RF radios), then $\theta_c = 732 \times 10^{-9}$. This can be converted now into the SSB signal-to-noise ratio:

$$£\left(f_m\right) = 20\log_{10}\frac{\theta_c}{2} = -128 \text{ dBc / Hz} \qquad \text{[Eq 7]}$$

The tuning diode adds significant noise, so if the above mentioned 1 kHz bandwidth for the PLL is used, at 2.4 kHz, the oscillator dominates.

Figure 3 shows the influence of the diode noise of a VCO at 150 MHz. In the case of lines B and C on the graph, you can see that the tuning diode greatly ruins the overall phase noise regardless of a high loaded *Q*!

The flicker frequency component also has a huge influence on the phase noise. Figure 4 shows the noise contribution of the flicker noise in a circuit with fixed *Q*. At 1 kHz offset, the phase noise deteriorates by 10 dB.

We can calculate the phase noise from circuit parameters, and using large singal parameters, or deriving these with the help from Bessel funtions, we specifically obtain Y21 for a large signal.

The total effect of all the four noise sources can be expressed as Equation 8.

$$\begin{aligned}
£\left(\omega\right) = {} & 10\log\frac{4KT}{\omega L \times Q}\left\{\frac{1}{2}\left[\frac{1}{2\omega_0 C_{eff}}\right]\left[\frac{\omega_0}{\omega}\right]\right\}^2_{\text{Resonator}} \\
& + 4KTr_b\left\{\frac{1}{2}\left[\frac{C_1+C_2}{C_2}\right]\left[\frac{1}{2Q}\right]\left[\frac{\omega_0}{\omega}\right]\right\}^2_{\text{Base Resistance}} \\
& + \left[2qI_b + \frac{2\pi K_f I_b^{AF}}{\omega}\right] \\
& \left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{2Q\omega_0 C_{eff}}\right]\left[\frac{\omega_0}{\omega}\right]\right\}^2_{\text{Flicker Base Current}} \\
& + 2qI_c\left\{\frac{1}{2}\left[\frac{C_1}{C_1+C_2}\right]\left[\frac{1}{2\omega_0 QC_{eff}}\right]\left[\frac{\omega_0}{\omega}\right]\right\}^2_{\text{Collector Current}}
\end{aligned} \qquad \text{[Eq 8]}$$

We will use the example from the 2 Part *Microwave & RF* article, "Large-Signal Approach Yields Low-Noise VHF/UHF Oscillators."[15,

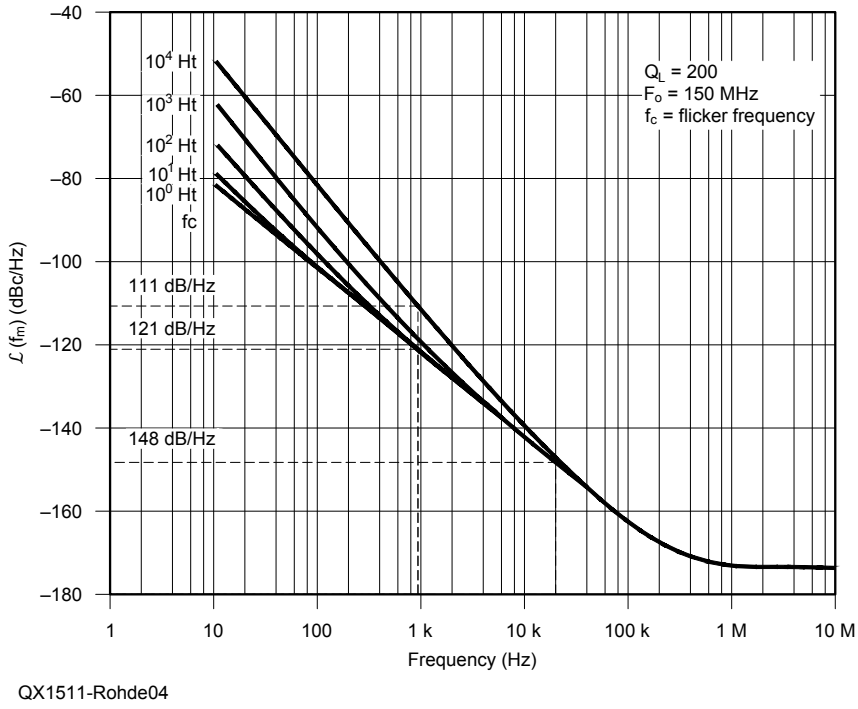


Figure 4 — Here is the phase noise contribution of the flicker noise to the oscillator noise.

[16] The schematic for this circuit is shown at Figure 5, and the measured phase noise of this 144 MHz oscillator is shown in Figure 6.

From the resonator, $R_P = 7056\ \Omega$ ($\omega L \times Q$)
Q of the resonator = 200 (Q of the inductor at 144 MHz)
Resonator inductance = 39 nH
Resonator capacitance = 22 pF
Collector current of the transistor, $I_c = 10$ mA
Base current of the transistor, $I_b = 85\ \mu$A
Flicker noise exponent, $AF = 2$
Flicker noise constant, $K_f = 1 \times 10^{-12}$
Feedback factor, $n = 5$
Phase noise at 10 kHz:

$$PN_{(ibn+ifn)_i}\left(\omega_0 + 10\text{ kHz}\right) \approx -134.2\text{ dBc / Hz}$$

$$PN_{Vbn}\left(\omega_0 + 10\text{ kHz}\right) \approx -151\text{ dBc / Hz}$$

$$PN_{nr}\left(\omega_0 + 10\text{ kHz}\right) \approx -169.6\text{ dBc / Hz}$$

$$PN_{icn}\left(\omega_0 + 10\text{ kHz}\right) \approx -150.6\text{ dBc / Hz}$$

$$P_{out} = 5\text{ dBm}$$

The value for $K_f = 1 \times 10^{-12}$ is vaild for small currents, and in Equation 8 the main phase noise (measured) contribution is the resonator loss. For higher frequencies and higher output power (higher DC current, the flicker and DC current contribuion to the flicker noise will dominate. At 30 mA and higher, a typcal K_f factor of 1×10^{-7} is common.

Going back to the large signal phase noise analysis , the Equation 9 is really the most modern result.

$$£(\omega) = 10\log\left\{\left[k_o + \left(\frac{k^3 k_1 \left[\frac{Y_{21}^+}{Y_{11}^+}\right]^2 [y]^{2p}}{\left[Y_{21}^+\right]^3 [y]^{3q}}\right)\left(\frac{1}{\left(y^2+k\right)}\right)\right]\left[\frac{(1+y)^2}{y^2}\right]\right\}$$

[Eq 9]

where:

$$k_0 = \frac{kTR}{\omega^2\omega_0^2 L^2 C_2^2 V_{cc}^2}$$

$$k_1 = \frac{qI_c g_m^2 + \frac{K_f I_b^{AF}}{4\omega} g_m^2}{\omega^2\omega_0^4 L^2 V_{cc}^2}$$

$$k_2 = \omega_0^4\left(\beta^+\right)^2$$

$$k_3 = \omega_0^2 g_m^2$$

$$k = \frac{k_3}{k_2^2 C_2^2}$$

where k_1, k_2, and k_3, are constant only for a particular drive level, with $y = C_1 / C_2$, making k_2 and k_3 also dependent on y, as the drive level changes.

This Equation is derived in *Communications Receivers* (see Note 8).

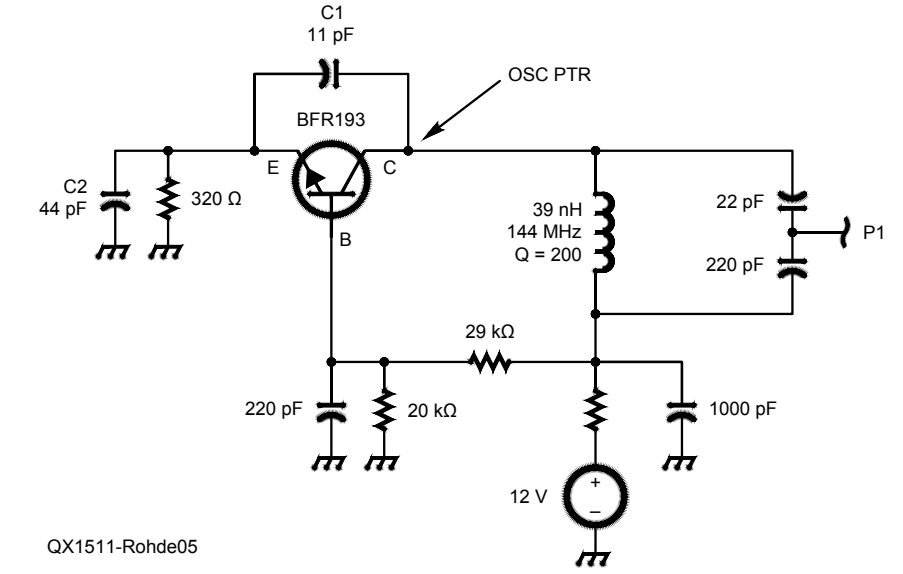


Figure 5 — This schematic shows a 144 MHz oscillator design at 60 MHz. This design is from "Large Signal Approach Yields Low-Noise VHF/UHF Oscillators," published in *Microwaves & RF*. See Notes 15 and 16.

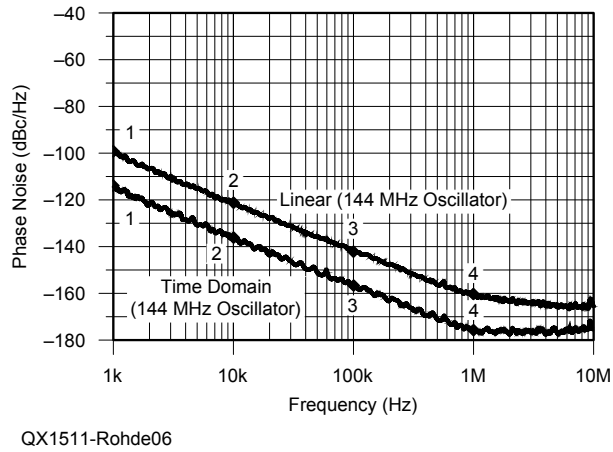


Figure 6 — This is the meassured phase noise of the 144 MHz Oscillator design of Figure 5, based on state of the art linear design, and based on an optimized design using large signal parameters. See Notes 15 and 16.

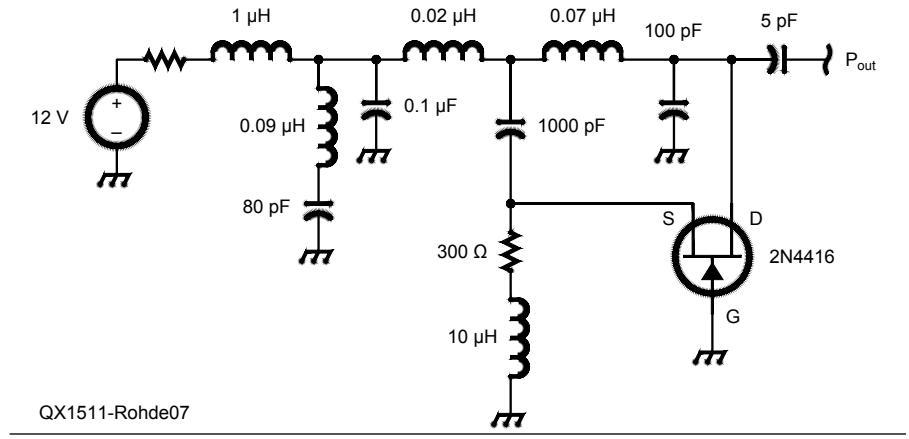


Figure 7 — This circuit is a possible simulation of the 60 MHz oscillator described by Colin Horrabin.

Another phase noise calculation approach is noted by Hajiimiri in "A General Theory of Phase Noise in Electrical Oscillators."[17] It is quoted by academicians frequently because it is an elegant way, but for actual design activities it is useless. It is mentioned here for completeness. Also see *The Design of Modern Microwave Oscillators for Wireless Applications: Theory and Optimization*.[18]

The Circuits

In order to verify the noise quoted by Colin Horrabin, an FET circuit with 2 tuned LC circuits was prepared for simulation using the familiar 2N4416 JFET. Its data was obtained from the non-linear data provided by Philips for CAD applications, such as *SPICE* or *Harmonic Balance* based simulators.[19]

The power supply voltage is applied via a 1 µH RF choke, and in order to validate the claim, the 0.1 µF capacitor in the analysis could be toggled between this value and 0.1 fF = 0.1 × 10^{-15} F, in practice a value of zero. The result showed no difference in phase noise. There was a discussion about why the simulator did not agree with the expectations, but the phase noise values published by Colin Horrabin did not support the claim either. This topic was addressed in the beginning of this paper. Interestingly enough, if the circuit is made asymmetrical (see the 80 pF and 100 pF capacitors in Figure 7), and the tap is not grounded, a better phase noise results.

The simulation data agree fairly well with the published data, and no correction for the noise of the tuning diode was made. Figure 8 shows the predicted phase noise of the Figure 7 oscillator.

It is now of interest to design a better VCO. This has been achieved with the design shown in Figure 9. The noise improvement comes from the constant current source (5.6 kΩ) in the source; the higher voltage drop is compensated by the positive voltage at the transistor gate.

Figure 10 shows a circuit diagram of an ultra low noise 60 MHz FET oscillator design that uses a 2N4416 FET. The circuit uses a helical resonator, as shown in Figure 11. The original cicuit was modified and is using six aditional diodes for a wider tuning range, and the parallel combination of the diodes, because of no noise correlation, results overall in a lower noise contribution. Figure 12 shows the phase noise simulation for this oscillator circuit, and Figure 13 shows the measured result from the actual circuit.

The diodes make the VCO noisier below 100 khz, but because the loop bandwidth typically is wider, this compensates the noise. If we look at Equation 8, we will find that

the major noise contribution is the loaded *Q* of the resonator. If by some magic the loading of the transistor drain impedance could be reduced, the noise would be less. Here, flicker noise is not the dominant cause!

Summary

The design of low noise oscillators is no longer such a mystical task. When I finally got my own R&S FSUP 8 with optimized internal signal sources, I went through the task of measuring my oscillators built 40 years ago, as well as some commercial devices. A good example was the older HP 8640B, and the famous HP 10544A 10 MHz crystal oscillators.

HP products typically were better than promised, something I could not claim for all of my designs, but I was not that far off — and yes some were better than published.

Sadly I found that many VHF crystal oscillators around in the past did not perform as well as we know today, and the same applies to signal generators.

This paper also lists a large number of references and I recommend *RF/Microwave Circuit Design for Wireless Applications* (see Note 2), *Microwave and Wireless Synthesizers: Theory and Design* (see Note 7), and *The Design of Modern Microwave Oscillators for Wireless Applications* (see Note 17) for text books for any readers interested in learning more about synthesizers and oscillators.

Microwave and Wireless Synthesizers: Theory and Design gives a detailed insight into PLL design, but companies now sell

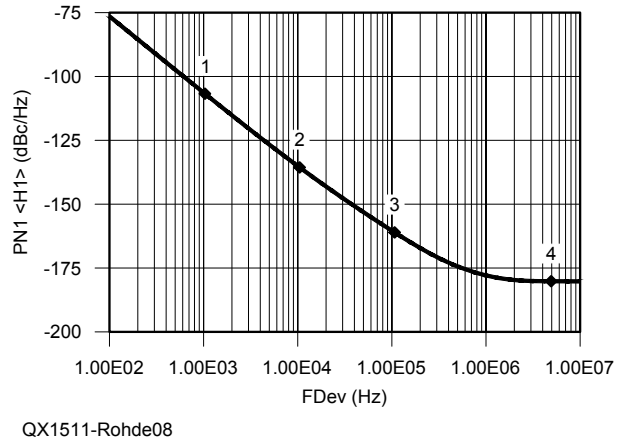


Figure 8 — This graph is the predicted phase noise of the Colin Horrabin oscillator, based on the simulation of Figure 7.

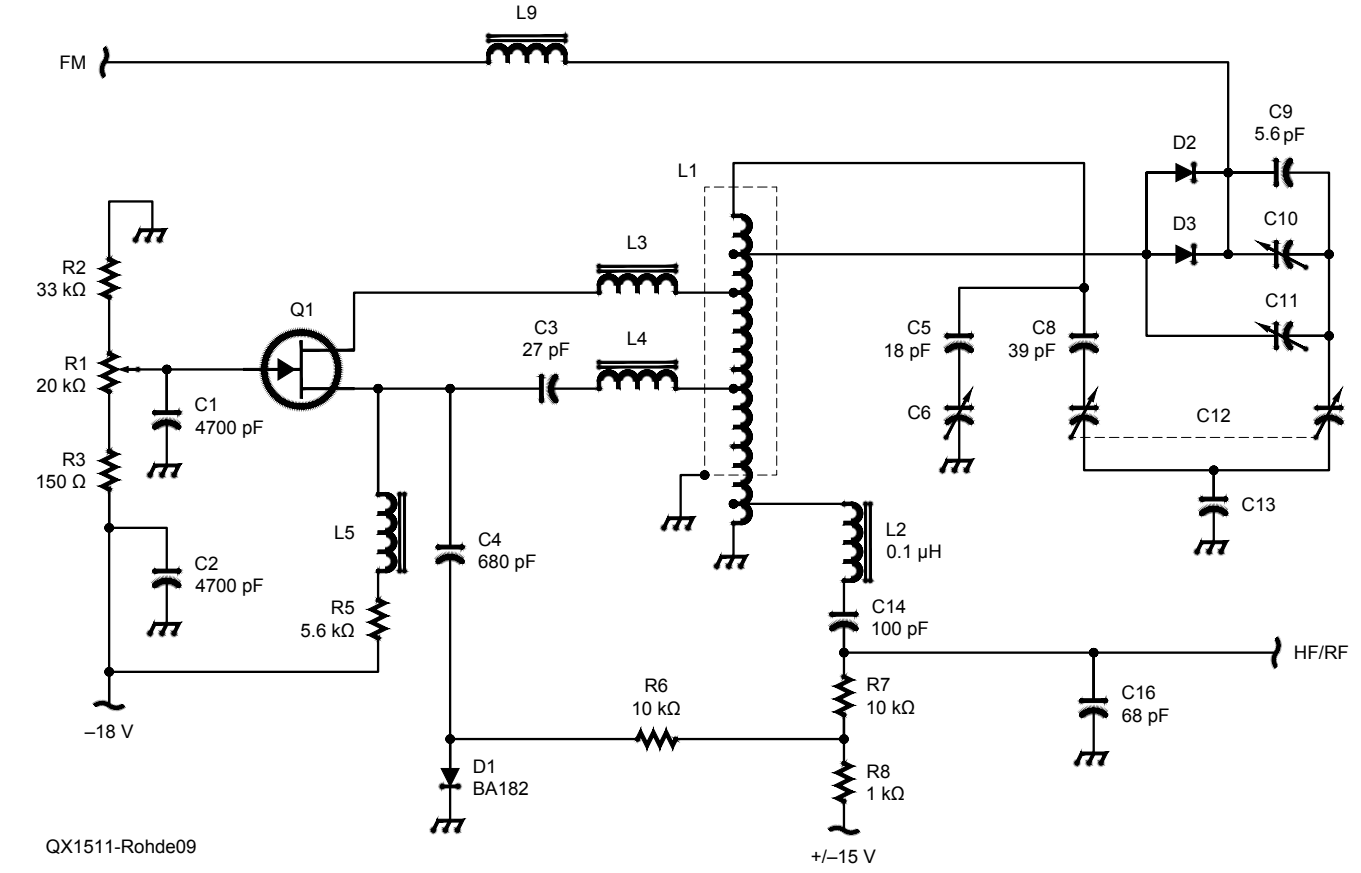


Figure 9 — This schematic diagram shows a 60 MHz VCO optimized for phase noise. It uses the 2N4416 FET and a ±15 V source, which switches the oscillator on and off. L1 is a helical resonator. R&S 1975 Model SMDU radio tester.

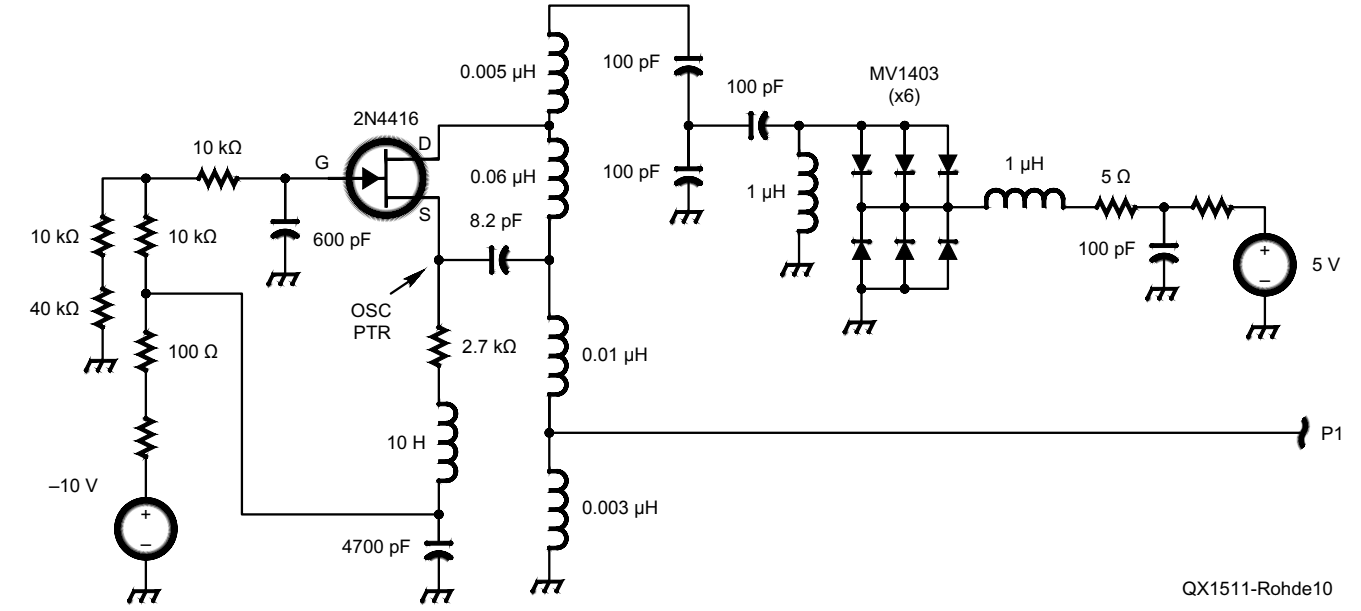


Figure 10 — Here is a typical circuit diagram of the 144 MHz low noise VCO using a 2N4416 FET. Note the six diodes for a wider tuning range of the oscillator. [R&S SMDU]

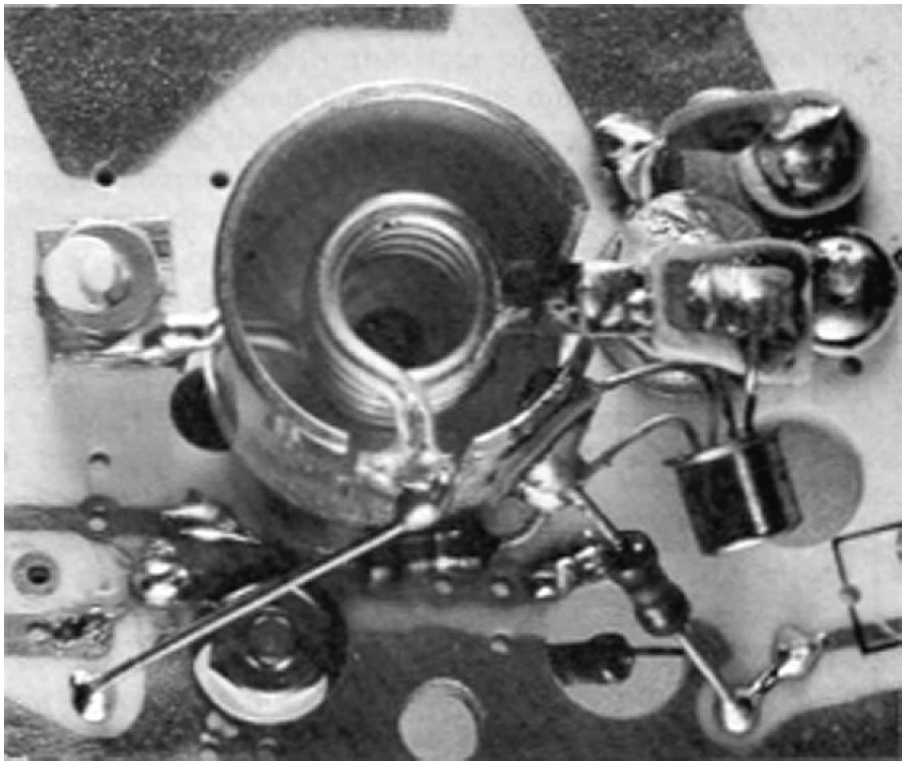


Figure 11 — This photo shows the helical resonator as part of the actual implementation of the oscilltor of Figure 9. Now the phase noise will be interesting. In practice, such an oscillator will have a buffer stage. The buffer stage will make the far off noise worse, so the result will be limited to about –165 dBc/Hz. This oscillator has an output level of 10 dBm (10 mW). The theoretical noise limit is 177 dB + 10 dB ≧ 187 dBc/Hz. The difference is due to the large signal noise figure of the transistor. [R&S SMDU]

complete PLL chips, so the individual designs disappear. Also the crystal chapter written by Roger Clark, then from Vectron, gives very valuable insight into this topic.

RF/Microwave Circuit Design for Wireless Applications, second edition, is a complete desk reference book, which also covers CMOS designs, and spends many pages on oscillators and CAD use.

The Design of Modern Microwave Oscillators for Wireless Applications addresses the very latest of wideband VCO design and push-push oscillators, and provides all the interesting phase noise calculations and design rules.

Based on the mathematics and design rules shown above, and good test equipment to validate the data, the design has become much easier.

As to the Horrabin oscillator, in one of his e-mails he mentioned a *Q* of 70 and the simulation supports that.

The improved oscillator above (no PLL!) at 3 kHz has a phase noise of –135 dBc/Hz while the Horrabin PLL design sits at –120 dBc/Hz. At higher frequencies the measured data published by Colin Horrabin supports a well-designed PLL based oscillator, but *not* any advantage of a symmetrical design. The practical designs above for a 144 MHz bipolar transistor based oscillator and this VCO gives some insight in good designs, both from a mathematical point and from a practical point.

Ulrich L. Rohde, N1UL, studied electrical engineering and radio communications at the Universities of Munich and Darmstadt, Germany. He holds a PhD in electrical engineering (1978) and a ScD (Honorary, 1979) in radio communications, a Dr-Ing (2004), University of Berlin, Germany in oscillator circuits and several honorary doctorates. In 2011 he earned a Dr-Ing Habil. Degree from the University of Cottbus, Germany.

He is President of Communications Consulting Corporation; Chairman of Synergy Microwave Corporation, Paterson, New Jersey; and a partner of Rohde & Schwartz, Munich, Germany. Previously he was President of Compact Software, Inc, Paterson, New Jersey; and Business Area Director for Radio Systems of RCA, Government Systems Division, Camden, New Jersey. He is a Professor of RF Microwave Circuit Design at Cottbus and has held Visiting Professorships at several universities in the United States and Europe.

Dr Rohde holds 25 patents and has published more than 200 scientific papers and has written or contributed to many books.

Dr Rohde is an ARRL Life Member, and is a Fellow of the IEEE, with positions on many IEEE Committees and Societies. In addition to his US call sign, he has held German call signs (DJ2LR/DL1R) since 1956 as well as Swiss call sign HB9AWE.

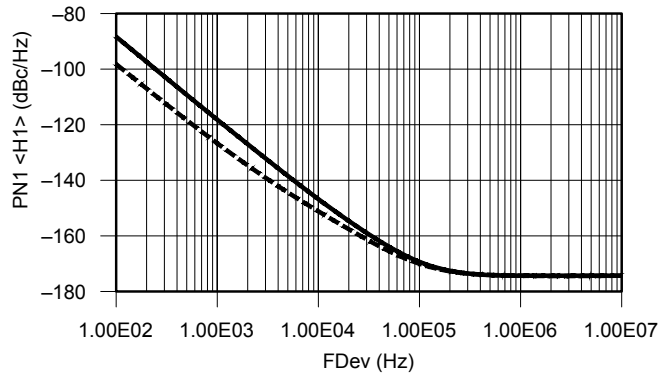


Figure 12 — Here is the phase noise simulation of the 60 MHz oscillator, using a helical resonator and tuning diodes.

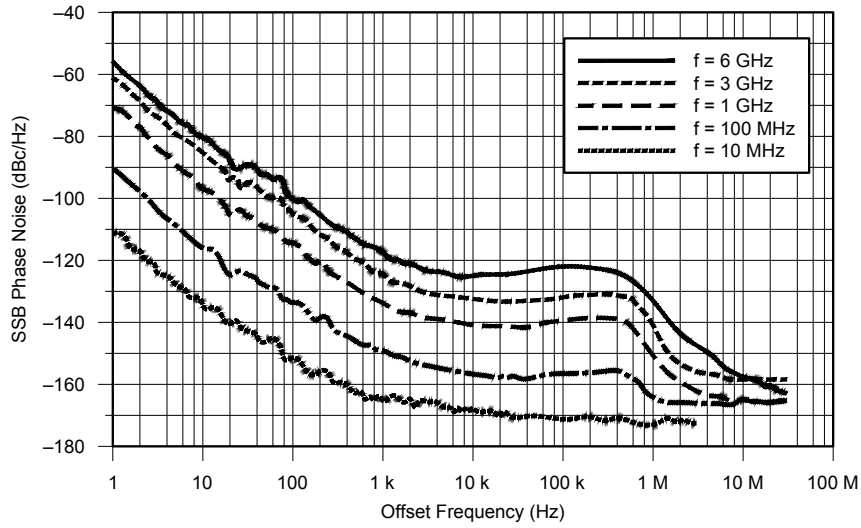


Figure 13 — Here is the measured phase noise of the oscillator of Figure 10, imbedded in a PLL system and multiplied up. For 60 MHz, the result would be between the lowest and second measured curve.

Notes

[1]Colin Horrabin, G3SBI, "The Development of the Low Phase Noise Double Tank Oscillator," Nov/Dec 2014 *QEX*, pp 35 – 43.

[2]Ulrich L. Rohde, N1UL, and Matthias Rudolph, *RF/Microwave Circuit Design for Wireless Applications*, Second Edition, John Wiley & Sons, 2013, ISBN 978-0-4-470-90181.

[3]Ulrich L. Rohde, N1UL, Juergen Schoepf, and Ajay K. Poddar, "Low-Noise VCOs Conquer Wide Bands", *Microwaves & RF*, pp. 98-106, June 2004.

[4]Ulrich L. Rohde, N1UL, and Ajay K. Poddar, "Noise Analysis of Systems of Coupled Oscillators," Integrated Nonlinear Microwave and Millimeter wave Circuits (INMMIC) workshop, Monte Porzo, Cantone, Italy, November 15-16, 2004.

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[10]Ulrich L. Rohde, KA2WEU, "Designing Low-Phase-Noise Oscillators," Oct 1004 *QEX*, pp 3 – 12. This article is available on the ARRL website at: **www.arrl.org/files/file/Technology/ard/rohde94.pdf**.

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[12]W. Anzill, F. X. Kärtner, and P. Russer, "Simulation of the Single-Sideband Phase Noise of Oscillators," Second International Workshop of Integrated Nonlinear Microwave and Millimeterwave Circuits, 1992.

[13]Dieter Scherer, "Design Principles and Test Methods for Low Phase Noise RF and Microwave Sources," RF & Microwave Measurement Symposium and Exhibition, Hewlett-Packard. This paper is available on line at: **www.am1.us/wp-content/Protected_Papers/U11604_Low_Noise_Sources-Scherer.pdf**.

[14]Enrico Rubiola, *Phase noise and Frequency Stability in Oscillators*, 2009, Cambridge University Press, ISBN 978-0521-15328-7.

[15]Ulrich L. Rohde, N1UL, and Ajay K. Poddar, "Large-Signal Approach Yields Low-Noise VHF/UHF Oscillators," *Microwaves & RF*, Part 1, April 2008, pp 62 – 76.

[16]Ulrich L. Rohde, N1UL, and Ajay K. Poddar, "Large-Signal Approach Yields Low-Noise VHF/UHF Oscillators," *Microwaves & RF*, Part 2, May 2008, pp 84 – 96.

[17]Ali Hajimiri and Thomas H. Lee, A General Theory of Phase Noise in Electrical Oscillators, IEEE Journal of Solid-State Circuits, Feb 1998, pp 179 – 194. This article is available on line at: **http://authors.library.caltech.edu/4917/1/HAJieeejssc98.pdf**.

[18]Ulrich L. Rohde, N1UL, Ajay K. Poddar, Georg Böck, *The Design of Modern Microwave Oscillators for Wireless Applications: Theory and Optimization*, John Wiley & Sons, 2005, ISBN: 978-0-471-72342-4.

[19]Harmonic Balance Simulator, Model - Serenade, by Ansys Corp., based on V. Rizzoli, F. Mastri, and D. Masotti, "General-Purpose Noise Analysis of forced Nonlinear Microwave Circuits," Military Microwave, 1992.

Using the MC1648 in Oscillators

The Motorola MC1648 is a specialized LC-oscillator IC that has been manufactured since the early 1970s and is a surviving member of MECL III, a long-obsolete family of emitter-coupled-logic devices. It is still used in military and commercial equipment. It is difficult to obtain, expensive, power hungry, and offers relatively low performance. Its circuitry is complex for an oscillator, with a multi-transistor limiting-amplifier cell controlled by an on-chip ALC system. The MC1648's first problem is that the ECL families use only about a 0.8 V swing between logic levels, and this same limitation applies to the signal in the oscillator tuned circuit. It is possible to improve this situation by using a tapped or transformer-coupled tank circuit to give improved Q, but risks the occurrence of the device's second problem: bandwidth creep.

Periodically, semiconductor manufacturers modernize their plants and scrap old assembly lines used to make old products. Any surviving devices then must undergo some redesign to allow continued production using the newer processes. One common result of this is that devices are shrunk, when possible, to fit more onto a wafer. All this increases the f_T of the transistors in the device, and such evolution has rendered today's MC1648s capable of operation at much higher frequencies than the specified 200-MHz limit. This allows higher-frequency use, of course, but great care is needed in the layout of circuits using it to prevent spurious oscillation. A number of old designs using this part have needed reengineering because the newer parts generate spurious oscillations that the old ones didn't, using PC-board traces as parasitic tuned circuits. Remember the Barkhausen criteria – as long as the gain is greater than 1 when phase shift is zero, there will be oscillation.

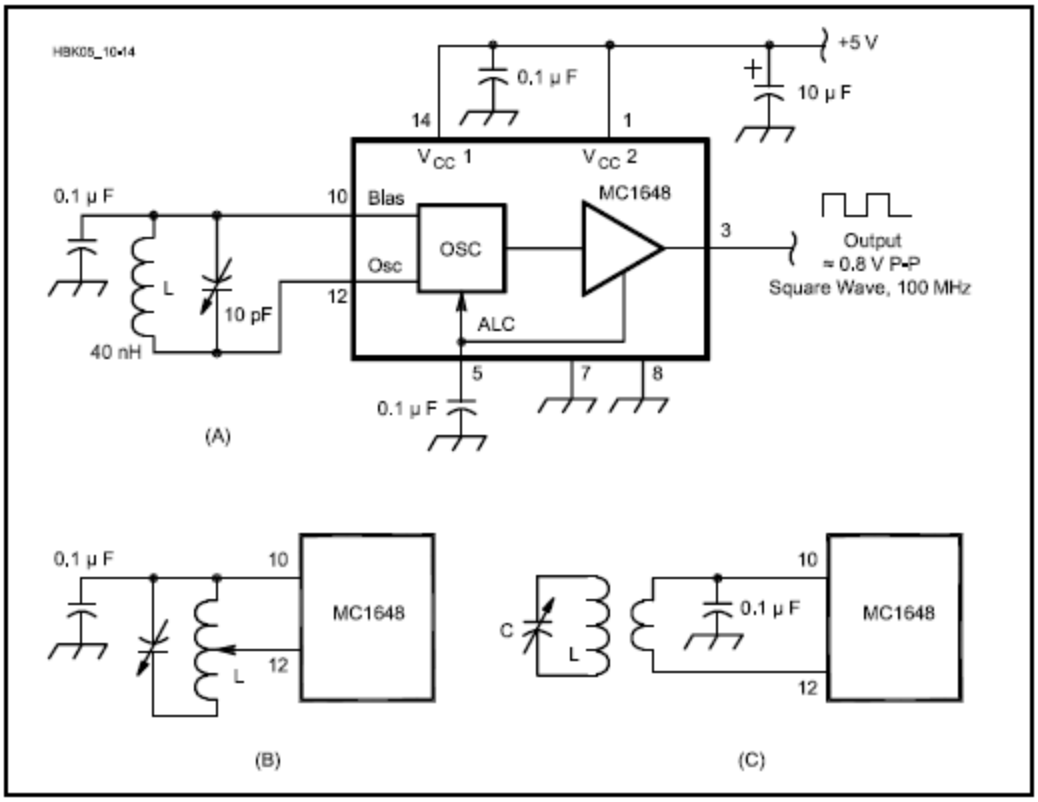

Figure 1 — One of the few ICs ever designed solely for oscillator service, the ECL Motorola MC1648 (A) requires careful design to avoid VHF parasitics when operating at HF. Keeping its tank Q high is another challenge; B and C show means of coupling the IC's low-impedance oscillator terminals to the tank by tapping up on the tank coil (B) or with a link (C).

The moral here is that a UHF-capable device always requires UHF-cognizant design and layout, even if the device is used at far lower frequencies. **Figure 1** shows the MC1648 in a simple circuit and with a tapped resonator. These more complex circuits have a greater risk of presenting a stray resonance within the device's operating range, risking oscillation at an unwanted frequency. This device is not a prime choice for an HF VFO because the physical size of the variable capacitor and the inevitable lead lengths, combined with the need to tap-couple to get sufficient Q for good noise performance, makes spurious oscillation difficult to avoid. The MC1648 is really intended for tuning-diode control in phase-locked loops operating at VHF.

This difficulty is inherent in all wideband devices, especially oscillator circuits connected to their tank by a single "hot" terminal, where there is simply no isolation between the amplifier's input and output paths. Any resonance in the associated circuitry can control the frequency of oscillation.

What you always wanted to know about Colpitts Oscillators

Ulrich L. Rohde[1, 2, 3] Anisha M. Apte[1]

1. Cottbus University BTU, Germany, 2. Technical University Munich (TUM), Germany, 3. University of Oradea, Romania

Introduction: Modern communications systems need oscillators as part of the design. In most cases these oscillators are part of a synthesizer and they are voltage controlled, meaning that the frequency is determined by tuning diodes, frequently called varactors. The applied DC voltage varies the frequency. For high performance circuits the Colpitts Oscillator is most frequently selected [1-30].

The Colpitts oscillator comes in three flavors – Figure 1a, shows the conventional circuit configuration. This type of circuit is based on a design developed by Edwin Henry Colpitts known for his invention of this oscillator and hence carries his name [1]. It uses a capacitive voltage divider and an inductor. In reality this simple circuit is not used but rather a derivation of this. This is shown in Figure 1b. The advantage of this circuit is that the values for C_1 and C_2 are fixed and the frequency change occurs by changing C_3. If the frequency of Figure 1a needs to be changed, a better choice is to vary the inductor L.

His colleague Ralph Hartley [2] invented an inductive coupling oscillator. The advantage of such an oscillator having capacitors C_1 and C_2 replaced with a tap of the inductor has been used together with helical resonators. The frequency tuning is achieved purely capacitively. To minimize loading, the transistor of choice here is a FET which has very high input impedance and provides minimum loading to the circuit. The disadvantage is that this circuit, using junction FETs, is limited to about 400 MHz. The transition frequency f_T is about 500MHz. FETs can also be used in the Colpitts oscillator as shown in Figure 1a, because of relatively lower loading than the bipolar transistor. The drawback of Figure 1a

is the heavy loading of the tuned circuit by the transistor. The circuit shown in Figure 1b is frequently referred to as the Clapp-Gouriet circuit [3].

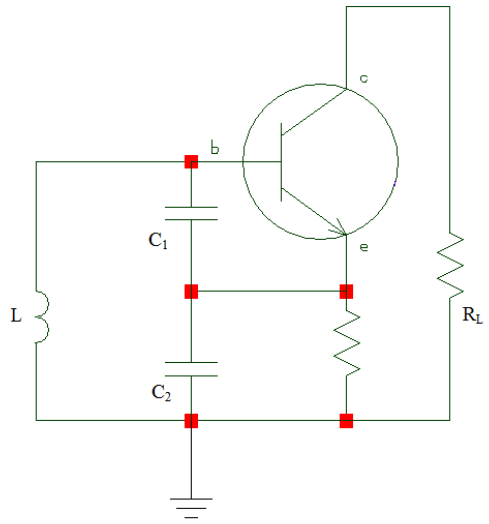

Figure 1a: Conventional Colpitts Configuration

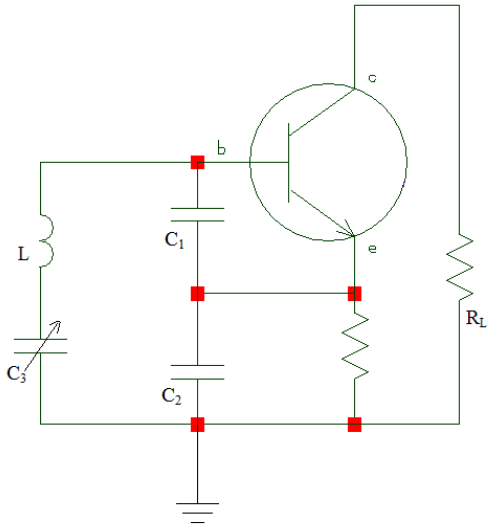

Figure1b: Modified Colpitts (Clapp-Gouriet) Config.

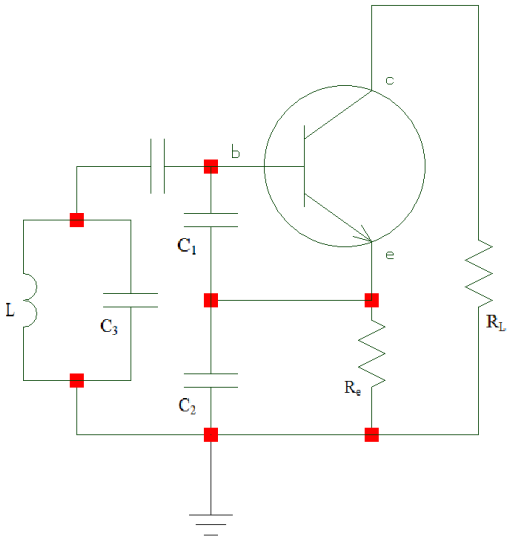

Figure 1c: Modified Colpitts Oscillator

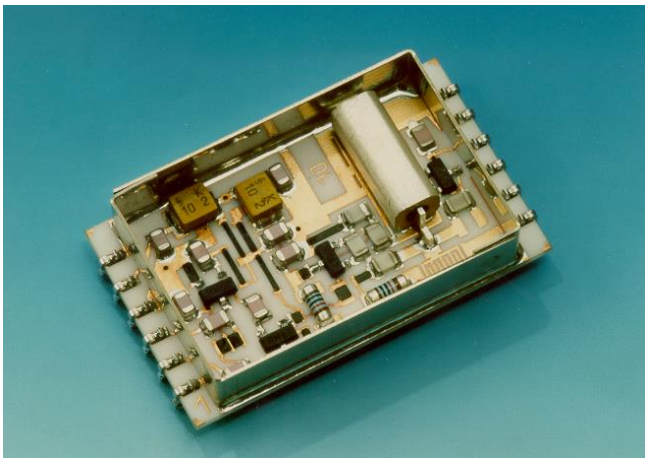

Figure 2: Photograph of 1 GHz CRO

At frequencies below 1GHz, both GaAs FETs and CMOS FETs are not a good choice because of their high flicker noise contribution.

For the circuit of Figure 1b, it is theoretically possible to have L and C_3 in resonance in which case the oscillator will cease to work. It is important to note here that the same circuit is used also for crystal oscillators; here the inductor L is replaced by the crystal. The crystal is a series combination of L_s, R_s and C_s with $Q = \omega L/R$. In practice the product of crystal Q and frequency is a constant. For 5 MHz, a typical Q of 2.5×10^6 is possible, resulting in a product of 12.5×10^{12}. If this is scaled to a crystal oscillator operating at 100MHz, the Q would be 125000. Manufacturers typically guarantee values greater than 100000.

Again, this crystal oscillator also falls into the category of Colpitts oscillator. A third variation is shown in Figure 1c. Here we have a parallel tuned circuit which is coupled loosely to the transistor. This circuit is found when building oscillators using ceramic resonators (CRO). Figure 2 shows such a design.

This paper summarizes the various methods of oscillator analysis and presents a step-by-step design procedure, showing the simulated, measured and calculated results for phase noise and other important parameters and concludes with a discussion on the effect of tuning diodes.

Linear Approach: For many years, until recently, oscillators were analyzed with a linear approach as will be shown below. Figures 3a and 3b illustrate the oscillator sub-circuit for the purpose of calculating the negative resistance.

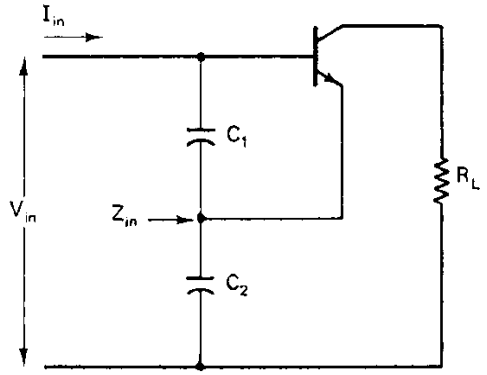

Figure 3a: Oscillator sub-circuit for impedance analysis

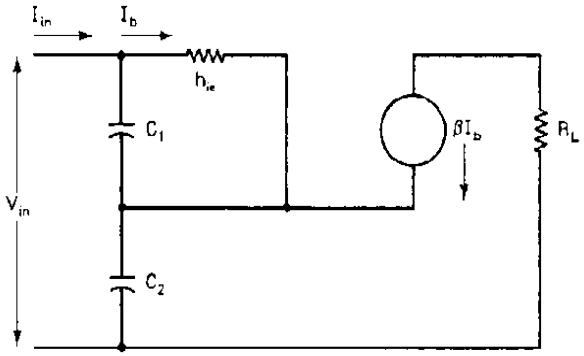

Figure 3b: Equivalent sub-oscillator circuit for the calculation of the negative resistance

From Figure 3b, the circuit equation is given from Kirchoff's voltage law (KVL) as

$$V_{\text{in}} = I_{\text{in}}\left(X_{C_1} + X_{C_2}\right) - I_b\left(X_{C_1} - \beta X_{C_2}\right) \tag{1a}$$

$$0 = -I_{\text{in}}\left(X_{C_1}\right) + I_b\left(X_{C_1} + h_{ie}\right) \tag{1b}$$

Considering, $\dfrac{1}{Y_{11}} = h_{ie}$

$$Z_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{(1+\beta)X_{C_1}X_{C_2} + h_{ie}\left(X_{C_1} + X_{C_2}\right)}{X_{C_1} + h_{ie}} \tag{1c}$$

$$Z_{\text{in}} = \frac{\left(-\dfrac{(1+\beta)}{\omega^2 C_1 C_2} + \dfrac{(C_1 + C_2)}{j\omega C_1 C_2}\dfrac{1}{Y_{11}}\right)}{\left(\dfrac{1}{Y_{11}} + \dfrac{1}{j\omega C_1}\right)} \tag{1d}$$

The input impedance (Z_{IN}) of this Colpitts Oscillator circuit, including the parasitics is given as [4, 5]:

$$Z_{IN}\big|_{pacakage} = -\left[\frac{Y_{21}}{\omega^2(C_1 + C_p)C_2}\frac{1}{(1+\omega^2 Y_{21}^2 L_p^2)}\right] - j\left[\frac{(C_1 + C_P + C_2)}{\omega(C_1 + C_P)C_2} - \frac{\omega Y_{21} L_P}{(1+\omega^2 Y_{21}^2 L_p^2)}\frac{Y_{21}}{\omega(C_1 + C_P)C_2}\right] \tag{2}$$

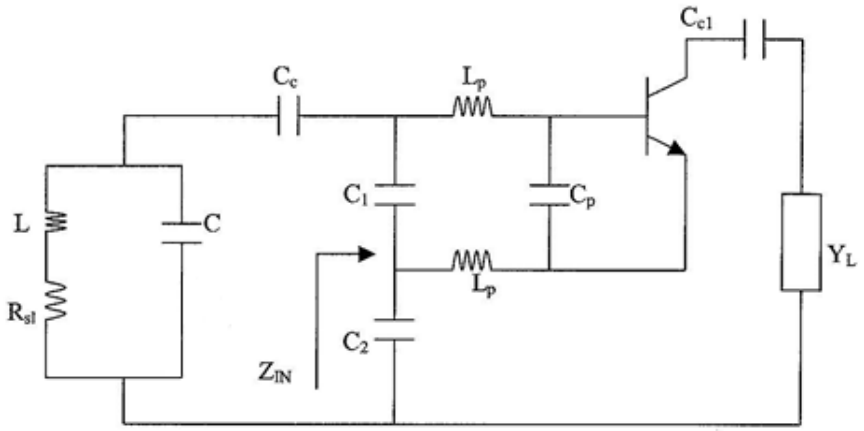

Figure 3c: Colpitts oscillator with base lead inductances and package capacitance

The resonator losses are expressed by the R_{s1}. Now splitting the Z_{IN} of the Colpitts oscillator into real and imaginary parts, including parasitics, we obtain,

$$R_{NEQ} = \frac{R_N}{(1+\omega^2 Y_{21}^2 L_p^2)} \tag{3}$$

$$\frac{1}{C_{EQ}} = \left\{ \left[\frac{1}{\frac{(C_1+C_P)C_2}{(C_1+C_2+C_P)}} \right] - \left[\frac{\omega^2 Y_{21} L_P}{(1+\omega^2 Y_{21}^2 L_P^2)} \right] \left[\frac{Y_{21}}{\omega(C_1+C_P)C_2} \right] \right\} \tag{4}$$

$$R_N = -\frac{Y_{21}}{\omega^2 C_1 C_2} \tag{5}$$

where

R_N : Negative resistance without lead inductance and package capacitance.

R_{NEQ} : Negative resistance with base-lead inductance and package capacitance.

C_{EQ} : Equivalent capacitance with base-lead inductance and package capacitance

The method shown above is called one-port oscillator design [6]. Figure 4 shows the general schematic diagram of a one-port negative-resistance model. The negative real part of Z_{IN} is used to compensate the losses of the parallel tuned circuit.

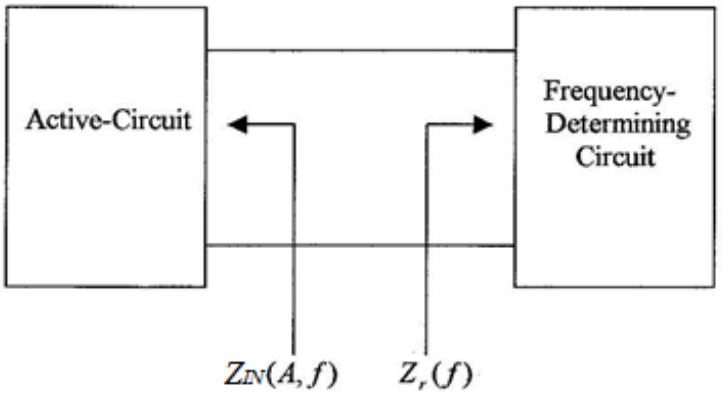

Figure 4: Schematic diagram of a one-port negative resistance model

Linear S-parameters approach:

It may be interesting for the readers to see how an oscillator can be analyzed using S-parameters. It should be noted that this method is based on linear approximations and works for practically all microwave oscillator designs [6, 28, pp-741]. The equivalent criteria of the negative resistance can be calculated in the form of S-parameters. The detailed definitions of S-parameters can be found in [31]. This negative resistance will cause oscillations if the following conditions are satisfied. Assume that the oscillation condition is satisfied at port 1 and is given by:

$$\frac{1}{S'_{11}} = \Gamma_G \tag{6}$$

Thus,
$$S'_{11} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} = \frac{S_{11}-D\Gamma_L}{1-S_{22}\Gamma_L} \tag{7}$$

$$\frac{1}{S'_{11}} = \frac{1-S_{22}\Gamma_L}{S_{11}-D\Gamma_L} = \Gamma_G \tag{8}$$

From expanding (7) we get

$$\Gamma_G S_{11} - D\Gamma_L\Gamma_G = 1 - S_{22}\Gamma_L \tag{9}$$

$$\Gamma_L(S_{22} - D\Gamma_G) = 1 - S_{11}\Gamma_G \tag{10}$$

$$\Gamma_L = \frac{1-S_{11}\Gamma_G}{S_{22}-D\Gamma_G} \tag{11}$$

$$S'_{22} = S_{22} + \frac{S_{12}S_{21}\Gamma_G}{1-S_{11}\Gamma_G} = \frac{S_{22}-D\Gamma_G}{1-S_{11}\Gamma_G} \tag{12}$$

$$\frac{1}{S'_{22}} = \frac{1-S_{11}\Gamma_G}{S_{22}-D\Gamma_G} \tag{13}$$

Comparing equations (9) and (12), we find that

$$\frac{1}{S'_{22}} = \Gamma_G \tag{14}$$

where, S_{11} and S_{22} are the input and output reflection coefficients, respectively

The discussion above means that the oscillation condition is also satisfied at port 2; which proves the simultaneous oscillation condition at both ports. Thus if either port is oscillating the other port must be oscillating as well. A load may appear at either or both ports, but normally the load is in Γ_L, the output termintation.

It is helpful to use the common-source based amplifier to compute the oscillator output power. For oscillators, the objective is to maximize ($P_{out} - P_{in}$) of the amplifier, which is the useful power to the load. An empirical expression for the common-source amplifier output power found by Johnson [29] is

$$P_{out} = P_{sat}\left(1 - exp\frac{-GP_{in}}{P_{sat}}\right) \tag{15}$$

Where P_{sat} is the saturated output power of the amplifier and G is the tuned small-signal common-source transducer gain of the amplifier, which is identical to $|S_{21}|^2$. Since the objective is to maximize (P_{out} - P_{in}), (where P_{out} and P_{in} are the output and input power of the amplifier),

$$d(P_{out} - P_{in}) = 0 \tag{16}$$

$$\frac{\partial P_{out}}{\partial P_{in}} = 1 \tag{17}$$

$$\frac{\partial P_{out}}{\partial P_{in}} = G_{exp} - \frac{GP_{in}}{P_{sat}} = 1 \quad (18)$$

$$exp\frac{GP_{in}}{P_{sat}} = G \quad (19)$$

$$\frac{P_{in}}{P_{sat}} = \frac{\ln G}{G} \quad (20)$$

At the maximum value of $(P_{out} - P_{in})$, the amplifier output is

$$P_{out} = P_{sat}(1 - \frac{1}{G}) \quad (21)$$

And the maximum oscillator output power is

$$P_{osc} = (P_{out} - P_{in}) \quad (22)$$

$$= P_{sat}\left(1 - \frac{1}{G} - \frac{\ln G}{G}\right) \quad (23)$$

Thus the maximum oscillator output power can be predicted from the common-source amplifier saturated output power and the small signal common source transducer gain G. For high oscillator output power high (loop) gain is of importance. Another definition of gain that is useful for large-signal amplifier or oscillator design is the maximum efficient gain, defined by

$$G_{ME} = \frac{P_{out} - P_{in}}{P_{in}} \quad (24)$$

For maximum oscillator power the maximum efficient gain from (20) and (21) is

$$G_{MEmax} = \frac{G-1}{lnG} \quad (25)$$

The RF gain G_{MEmax} is a considerably smaller value compared to G, the small-signal gain [7-12].

Designing oscillators based on S-parameters in a linear mode has been quoted by many authors using first approximation for large signal as shown in [8]. The problem with this published approach is that it uses a GaAs FET, where only the transconductance g_m has a major influence. S_{11} changes very little under large signal conditions, as does S_{22}. Reliable large signal S-parameters for bipolar transistors and FETs are difficult to get.

Time-domain based analysis to analyze the transistor non-linarities':

A correction for the frequency dependent parameters will follow, based on "simulation" for larger drive level.

The voltage $v(t)$ across the base-emitter junction consists of a DC component and a driven signal voltage $V_1 \cos(wt)$. It can be expressed as

$$v(t) = V_{dc} + V_1 \cos(wt) \tag{26}$$

As the driven voltage $V_1 \cos(wt)$ increases and develops enough amplitude across the base-emitter junction, the resulting current is a periodic series of pulses whose amplitude depends on the nonlinear characteristics of the device and is given as

$$i_e(t) = I_s e^{\frac{qv(t)}{kT}} \tag{27}$$

$$i_e(t) = I_s e^{\frac{qV_{dc}}{kT}} e^{\frac{qV_1 \cos(wt)}{kT}} \tag{28}$$

$$i_e(t) = I_s e^{\frac{qV_{dc}}{kT}} e^{x\cos(wt)} \tag{29}$$

assuming $I_c \approx I_e$ (β>10)

$$x = \frac{V_1}{(kT/q)} = \frac{qV_1}{kT} \tag{30}$$

$i_e(t)$ is the emitter current and x is the drive level which is normalized to kT/q.

From the Fourier series expansion, $e^{x\cos(wt)}$ is expressed as

$$e^{x\cos(wt)} = \sum_n a_n(x)\cos(nwt) \tag{31}$$

$a_n(x)$ is a Fourier coefficient and given as

$$a_0(x)\big|_{n=0} = \frac{1}{2\pi}\int_0^{2\pi} e^{x\cos(wt)}d(wt) = I_0(x) \tag{32}$$

$$a_n(x)\big|_{n>0} = \frac{1}{2\pi}\int_0^{2\pi} e^{x\cos(wt)}\cos(nwt)d(wt) = I_n(x) \tag{33}$$

$$e^{x\cos(wt)} = \sum_n a_n(x)\cos(nwt) = I_0(x) + 2\sum_1^{\infty} I_n(x)\cos(nwt) \tag{34}$$

$I_n(x)$ is the modified Bessel function.

$$\text{As } x \to 0 \Rightarrow I_n(x) \to \frac{(x/2)^n}{n!} \tag{35}$$

$I_0(x)$ are monotonic functions having positive values for x≥0 and n≥0; $I_0(0)$ is unity, whereas all higher order functions start at zero.

The short current pulses are generated from the growing large-signal drive level across the base-emitter junction, which leads to strong harmonic generation [5, 27]. The advantage of this pulse performance is the reduction of phase noise, due to the smaller duty cycle of the transistor [4]. The emitter current represented above can be expressed in terms of harmonics as

$$i_e(t) = I_s e^{\frac{qV_{dc}}{kT}} I_0(x)\left[1 + 2\sum_1^{\infty}\frac{I_n(x)}{I_0(x)}\cos(nwt)\right] \tag{36}$$

$$I_{dc} = I_s e^{\frac{qV_{dc}}{kT}} I_0(x) \tag{37}$$

$$V_{dc} = \frac{kT}{q}\ln\left[\frac{I_{dc}}{I_s I_0(x)}\right] \Rightarrow \frac{kT}{q}\ln\left[\frac{I_{dc}}{I_s}\right] + \frac{kT}{q}\ln\left[\frac{1}{I_0(x)}\right] \tag{38}$$

I_s = collector saturation current

$$V_{dc} = V_{dcQ} - \frac{kT}{q} \ln I_0(x) \tag{39}$$

$$i_e(t) = I_{dc}\left[1 + 2\sum_{1}^{\infty} \frac{I_n(x)}{I_0(x)} \cos(nwt)\right] \tag{40}$$

V_{dcQ} and I_{dc} are the operating DC bias voltage and the DC value of the emitter current. Furthermore, the Fourier transform of $i_e(t)$, a current pulse or series of pulses in the time domain yields a number of frequency harmonics common in oscillator circuit designs using nonlinear devices.

The peak amplitude of the harmonic content of the output current is defined as $\left[\frac{I_N(x)}{I_1(x)}\right]$, and the DC offset voltage are calculated analytically in terms of the drive level, as shown in Table 1. It gives good insight of the nonlinearities involved in the oscillator design.

Table 1: For T=300 K, data are generated at a different drive–level

Drive level [x]	Drive-Voltage $\left(\left[\frac{kT}{q}\right] * x\right)$mV	Offset-Coefficient ln[I_0(x)]	DC-Offset $\frac{kT}{q}[\ln I_0(x)]$ mV	Fundamental Current 2[I_1(x)/I_0(x)]	Second-Harmonic [I_2(x)/I_1(x)]
0.00	0.000	0.000	0.000	0.000	0.000
0.50	13.00	0.062	1.612	0.485	0.124
1.00	26.00	0.236	6.136	0.893	0.240
2.00	52.00	0.823	21.398	1.396	0.433
3.00	78.00	1.585	41.210	1.620	0.568
4.00	104.00	2.425	63.050	1.737	0.658
5.00	130.00	3.305	85.800	1.787	0.719
6.00	156.00	4.208	206.180	1.825	0.762
7.00	182.00	5.127	330.980	1.851	0.794
8.00	208.00	6.058	459.600	1.870	0.819
9.00	234.00	6.997	181.922	1.885	0.835
10.00	260.00	7.943	206.518	1.897	0.854
15.00	390.00	12.736	331.136	1.932	0.902

20.00	520.00	17.590	457.340	1.949	0.926

It may be of interest to see the start-up condition of an oscillator; the transient response is shown in Figure 5.

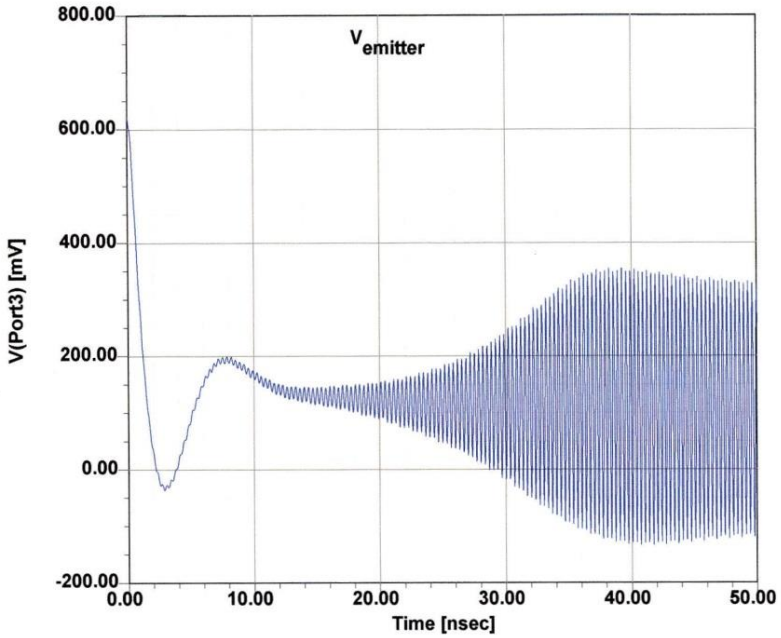

Figure 5: Example of the transient simulation of a ceramic resonator based high-Q oscillator showing the DC-offset as shown in column 4, Table 1 (The voltage displayed is taken from the emitter)

Selecting the right transistor:

The basic design of a Colpitts oscillator is the same, whether one uses a FET or BJT. Bipolar transistor based oscillators can now easily be designed up to 20GHz. The basic advantage of the bipolar transistor (also known as BIP) is the lower flicker noise corner frequency. Currently transistor chips with F_{max} up to 300GHz are available in the foundry environment, commercially up to about 150GHz. For the purpose of this design synthesis, we have decided to use a BFG520, which is a highly linear transistor. It is validated with a 3-tone test (the typical 2-tone test is easier to meet), as found from the

datasheet; the mixing products are better than -60dB suppressed relative to the carrier. Based on past experience for its good linearity, the BFG520 also has low distortion and, low noise. The key parameters are V_{CEO} = 15V, I_c = 70mA, P_{tot} = 300mW, Noise Figure F_{min} at 350MHz is less than1dB, at 5mA, the associated gain is more than 17dB.

A Design Example for a 350MHz fixed frequency Colpitts Oscillator

The following is an exact mathematical solution for designing the 350MHz Colpitts Oscillator.

The circuit consists of the Colpitts configuration following Figure 1c. In order to have enough loop gain, a microwave transistor BFG520 is used. At the proposed starting DC current of 6mA, (being close to the minimum noise figure current and as a first trial to meet the output power), f_T is 6GHz. When selecting a transistor with a higher f_T there is always a possibility of unwanted microwave oscillation and higher flicker noise. When comparing microwave transistors with audio transistors, it becomes apparent that at much lower frequencies there is much less flicker noise contribution. This transistor can safely be operated at 30mA but the rule of thumb is, when using 10% to 15% of Ic_{max}, the flicker contribution is much less. For low noise operation, the datasheet indicates 1.1dB spot noise figure at 900MHz at 5mA.

The 350 MHz oscillator, using the bipolar transistor BFG520, is designed based on analytical equations and is later verified with simulation results. Based on the output power requirement and harmonics at a given load, the drive level is fixed. The normalized drive level (of x = 15) is chosen to allow adequate drive level to sustain oscillation and yet, not to produce excessive harmonic content. Figure 6, shows the values of the optimized circuit. While simulating for a series resonant configuration, the value of C_p = 8.2fF, was used as a place-holder, based on impedance considerations. C_p was set to 8.2pF for parallel resonant configuration, the value of L = 21nH, and C_c = 3.3pF was set

to achieve oscillation at 350MHz. Experimenting with the simulation, it turns out that 'L_b' set to 0.5uH gives a much better phase noise, about 10dB better at 100Hz offset, but this could not be verified yet in a real circuit.

The output power is taken from the collector and following is the design procedure. The goal is to obtain an output power over 10dBm, using a simple design for good understanding.

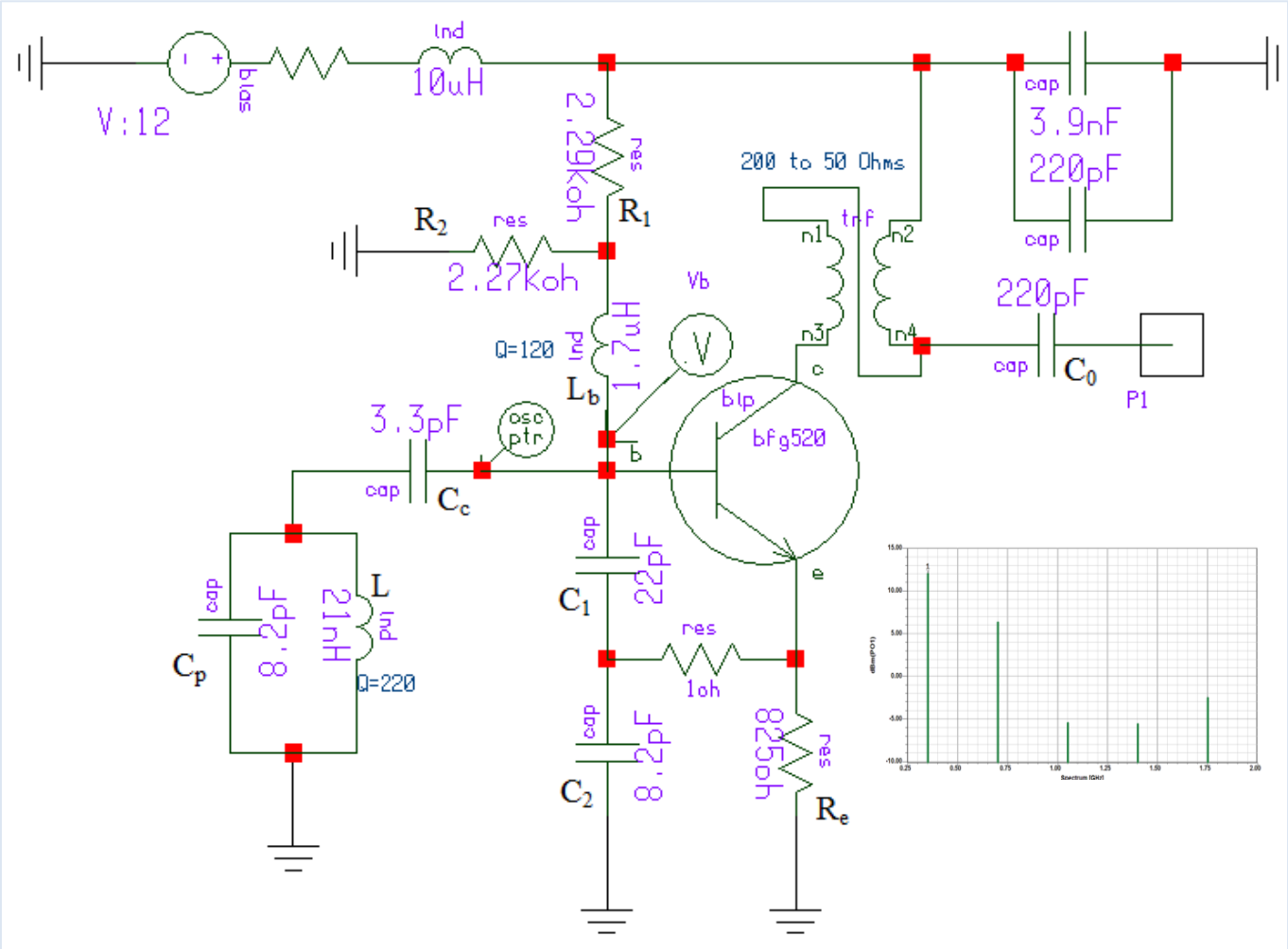

Figure 6: Design of 350MHz Colpitts Oscillator – Optimized for phase noise

Step 1:

The normalized drive level will be set at 15, for which the fundamental peak current

I_1 *(fundamental)* = $1.932 I_{dc}$ (is given from table 1).

I_1 is the fundamental current specified by the output power needed for the designated load.

The primary impedance of the transformer is 200Ω and we calculate the RF voltage for $R_L = 200\Omega$ and for a output power of $P_{out} \approx 11$ dBm ≈ 14mW

$V_{out} = \sqrt{P_{out}(mW) \times 2R_L} = \sqrt{14 \times 10^{-3} \times 2 \times 200} = 2.37V$ (No saturation voltage assumed! This results in slight variation between calculated, simulated and measured values of Pout.) (41)

$$I_1 = \frac{V_{out}}{200} = \frac{2.37}{200} \cong 11.85mA \quad (42)$$

$$I_e = I_{dc} = \frac{I_1}{1.932} = \frac{11.85}{1.932} = 6.13mA \quad (43)$$

Step 2: Biasing

The transistor uses a 12V power supply and an 825Ω emitter resistor at ~6mA, resulting in ~5V drop, so the transistor can afford a large voltage swing between base and ground. This reduces flicker noise (resistive feedback) and distortion. The base voltage divider, for reasons pertaining to temperature stability uses a higher than normal dc current, is isolated from the base using a RF choke. Frequently, in designs, this circuit trick is not used.

$$V_b = I_e \left[R_e + \frac{R_e}{\beta + 1} \right] + V_{be} = 5.96V \quad (44)$$

β is assumed to be around 100 and V_{be} is approximately 0.8V.Bias resistor R_1 and R_2 is given as

$$V_b = \frac{R_2}{R_1 + R_2} V_{cc} = 5.96V \Rightarrow \frac{R_1}{R_2} \approx 1 \quad (45)$$

$$R_1 = 2270\Omega \tag{46}$$

$$R_2 = 2290\Omega \tag{47}$$

$$V_{cc} = 12V \tag{48}$$

Resistor Bias current is ~2.6mA ($V_{cc}/(R_1+R_2)$)

Base current is 43μA, so the safety factor is $2.6/0.043 \cong 60$

Step 3: Determination of the large signal transconductance

Based on the table above, and x=15, the "DC transconductance" equals

$$Y_{21} = \left.\frac{I_1}{V_1}\right|_{fundamental-freq} = \frac{1.932 I_{dc}}{1000mV} = \frac{11.85mA}{1000mV} \cong 12mS \tag{49}$$

This is the DC transconductance, meaning the frequency dependence has not been considered.

An analysis of the transistor shows that the small signal transconductance at 6mA (dc) is about 6×39 ≈ 240mS. At 350MHz this reduces itself to 200mS down from 240mS. This is valid only if the transistor does not have any emitter feedback. In the case of the Colpitts oscillator we have an emitter resistor which reduces the transconductance; therefore we have to multiply Y_{21} with

$$\left(\frac{1}{(1/g_m) + R_e}\right) \tag{50}$$

The resulting large signal loop transconductance Y_{21L} is $\frac{1}{(\frac{1}{12\times10^{-3}}) + 825)} \cong 1.1mS$, which is an acceptable approximation, as the exact value of x is about 20 (see simulation results, Figure 9) [Ref. 26, pg.177].

Based on Kirchhoff's law, the following set of equations can be used to determine the feedback factor 'n'.

$Y_{21L} = 1.1mS$ (DC Transconductance – No high frequency effects included) where $\alpha = 0.99$

The oscillator circuit with passive component parameters is shown in Figure 7a.

Table 2: Large signal transconductance as a function of Drive level based on Bessel function Calculations - $G_m(x)/g_m=2[I_1(x)/xI_0(x)]$ vs. the drive level = x.

Drive level: x	$G_m(x)/g_m=2[I_1(x)/xI_0(x)]$
0.00	1
0.50	0.970
1.00	0.893
2.00	0.698
3.00	0.540
4.00	0.432
5.00	0.357
6.00	0.304
7.00	0.264
8.00	0.233
9.00	0.209
10.00	0.190
15.00	0.129
20.00	0.0975
25.00	0.075

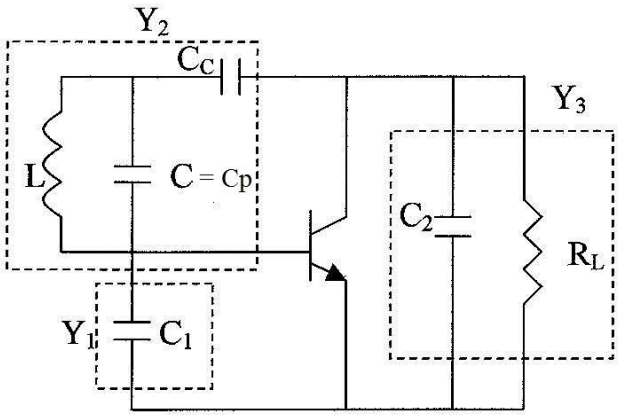

Figure 7a: Oscillator circuit with the passive components Y_1, Y_2, and Y_3

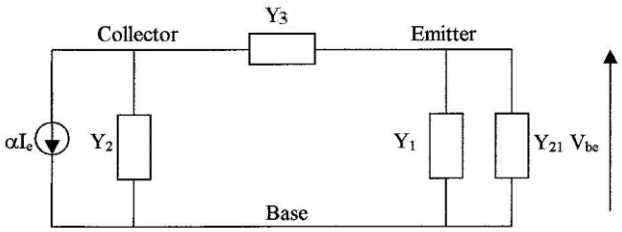

Figure 7b: Equivalent oscillator circuit for the analysis of the transformed conductance seen by the

current source

Where,

$$Y_1 = G_1 + jB_1 \Rightarrow j\omega C_1 \text{ For } G_1 = 0 \quad (51\text{-a})$$

$$Y_2 = G_2 + jB_2 \Rightarrow G_2 + j\left[\frac{(\omega^2 LC - 1)\omega C_c}{\omega^2 L(C_c + C) - 1}\right]; \quad (51\text{-b})$$

G_2 = loss parameter/load conductance of the resonator connected parallel to the resonator component C_1, C_2 and L, respectively.

$$Y_3 = G_3 + jB_3 \Rightarrow G_3 + j\omega C_2; \quad (51\text{-c})$$

G_3 = conductance of the bias resistor placed across C_2, $1/R_L$ in Figure 7a.

The large-signal transconductances Y_{21} and G_1 are transformed to the current source through the voltage divider $\frac{V_{eb}}{V_{cb}}$. The voltage V_{eb} must be added to V_{ce} to calculate the transformation ratio, which is also inverse of the feedback factor and can be written as $\frac{V_{eb}}{V_{cb}} = \frac{C_2}{C_1 + C_2} = \frac{1}{n}$ (51-d)

And $\frac{V_{ce}}{V_{cb}} = \frac{C_1}{C_1 + C_2} = \frac{n-1}{n}$ (51-e)

The conductance G_2 is already in parallel with the current source so it remains unchanged. The factor "n" represents the ratio of the collector-base voltage to the emitter-base voltage at the oscillator resonant frequency.

$$G_1 \rightarrow \frac{G_1}{n^2} \quad (51\text{-f})$$

$$Y_{21} \rightarrow \frac{Y_{21}}{n^2} \Rightarrow \frac{G_m}{n^2} \tag{51-g}$$

$$G_3 \rightarrow \left[\frac{n-1}{n}\right]^2 G_3 \tag{51-h}$$

G_2 remains constant

The transformed conductance is proportional to the square of the voltage ratios given in Equations (51-d) and (51-e), producing a total conductance as seen by the current source at resonance as

$$G_{total} = G_2 + \frac{G_m + G_1}{n^2} + \left[\frac{n-1}{n}\right]^2 G_3 \tag{51-i}$$

For sustained oscillation, the closed loop gain at resonance is given as

$$\left[\frac{\left(\frac{V_{be} Y_{21} \alpha}{nG_{total}}\right)}{V_{be}}\right] = 1 \Rightarrow nG_{total} = Y_{21}\alpha \tag{51-j}$$

$$\frac{Y_{21}}{nG_{total}} = \frac{1}{\alpha} \Rightarrow \frac{Y_{21}}{nG_{total}} > 1 \tag{51-k}$$

α is assumed to be 0.0.99 and variation in the value of α does not influence the expression above greatly. Rearranging the device conductance and circuit conductance, the general oscillator equation, after multiplying (51-i) with *n* on both sides, is written as

$$nG_{total} = n\left[G_2 + \frac{Y_{21} + G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \tag{51-l}$$

$$Y_{21}\alpha = n\left[G_2 + \frac{Y_{21} + G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \Rightarrow \left[\frac{-(1-n\alpha)}{n^2}\right] Y_{21} = \left[G_2 + \frac{G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \tag{51-m}$$

$$n^2(G_2+G_3)-n(2G_3+Y_{21}\alpha)+(G_1+G_3+Y_{21})=0 \tag{51-n}$$

$$n=\frac{(2G_3+Y_{21}\alpha)\pm\sqrt{(2G_3+Y_{21}\alpha)^2-4(G_2+G_3)(G_1+G_3+Y_{21})}}{2(G_2+G_3)} \tag{51-o}$$

$$n_1=\frac{(2G_3+Y_{21}\alpha)}{2(G_2+G_3)}+\frac{\sqrt{(2G_3+Y_{21}\alpha)^2-4(G_2+G_3)(G_1+G_3+Y_{21})}}{2(G_2+G_3)} \tag{51-p}$$

$$n_2=\frac{(2G_3+Y_{21}\alpha)}{2(G_2+G_3)}-\frac{\sqrt{(2G_3+Y_{21}\alpha)^2-4(G_2+G_3)(G_1+G_3+Y_{21})}}{2(G_2+G_3)} \tag{51-q}$$

From the quadratic equation above, the value of the factor n can be calculated, and thereby, an estimation of the capacitance can be done a priori.

To ensure higher loop gain, n_1 is selected from $n_{max}[n_1, n_2]$.

Once the value of n is fixed, then the ratio of the capacitance is calculated as

$$\frac{C_2}{C_1+C_2}=\frac{1}{n} \tag{51-r}$$

$$C_2=\frac{C_1}{n-1}\Rightarrow\frac{C_1}{C_2}=n-1 \tag{51-s}$$

If G_3 and G_1 are zero then the quadratic equation (51-n) reduces to

$$n^2G_2-nY_{21}\alpha+Y_{21}=0 \tag{51-t}$$

$$Y_{21}\cong\frac{n^2}{1-n}G_2\Rightarrow Y_{21}=\left[\frac{n^2}{1-n}\right]\frac{1}{R_P} \tag{51-u}$$

$$\frac{Y_{21}R_P}{n}=\frac{n}{1-n} \tag{51-v}$$

$$R_P=\frac{1}{G_2},\qquad \frac{Y_{21}R_P}{n}\rightarrow Loop\ Gain \tag{51-w}$$

$$\textit{Loop Gain}\ \ \frac{Y_{21}R_P}{n} \to 1 \tag{51-x}$$

From equation (51-r) and (51-u)

$$Y_{21} \Rightarrow G_m(x) = \frac{1}{R_P}\frac{[C_1 + C_2]^2}{C_1 C_2} \tag{51-y}$$

The quadratic equation for *n* (from (51-n)) is reduced to

$$n^2(G_3) - n(2G_3 + Y_{21}\alpha) + (G_3 + Y_{21}) = 0 \tag{52-a}$$

$$G_3 = \frac{1}{R_e} = \frac{1}{825} = 1.21mS$$

$$n^2(1.21) - n(2\times 1.21 + 1.1\times 0.99) + (1.21 + 1.1) = 0 \tag{52-b}$$

$$1.21n^2 - 3.514n + 2.313 = 0 \tag{52-c}$$

$$n = \frac{3.514 \pm \sqrt{(3.514)^2 - 4\times 1.21\times 2.313}}{2\times 1.21} \tag{53}$$

$$n \Rightarrow n_1 = 1.888 and\ n_2 = 1.01 \tag{54}$$

The higher value of the transformation factor, *n*, is selected as *n* = 1.888.

The ratio for the values of C_1 and C_2 is calculated as

$$\frac{C_2}{C_1 + C_2} = \frac{1}{n} \Rightarrow C_2 = \frac{C_1}{n-1} \tag{55}$$

$$C_2 = \frac{C_1}{n-1} = \frac{C_1}{0.888} \Rightarrow \frac{C_1}{C_2} \cong 0.9 \approx 1 \tag{56}$$

The ratio of the capacitor C_1 to C_2 is 1. For larger transconductance, Y_{21}, $(C_1/C_2) > 1$

A discussion about drive level and noise:

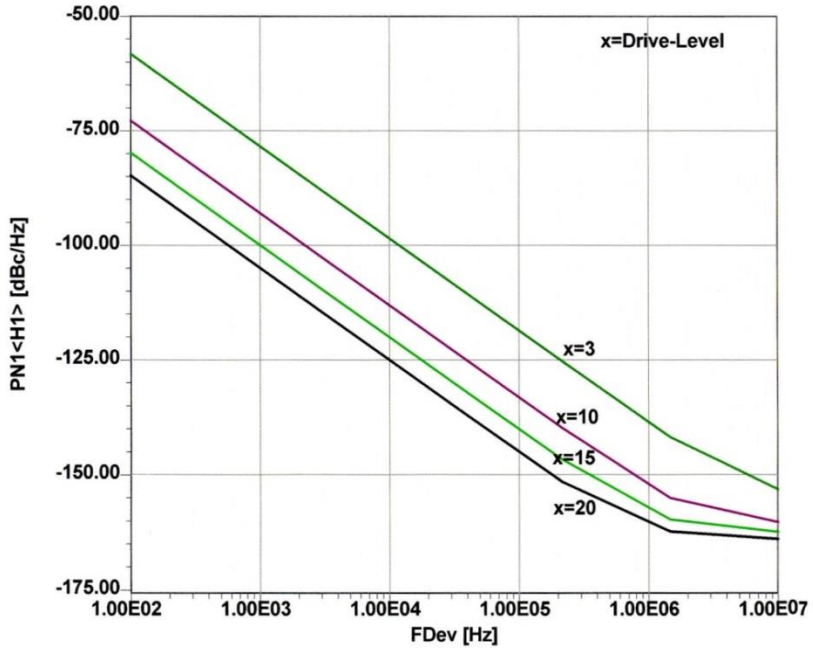

Figure 8: Example for the single sideband phase noise as a function of the normalized drive level x for a high Q 1GHz oscillator

The plot in Figure 8 [5] shows the impact of the normalized drive level 'x' on the phase noise. The exact values have to be assessed for individual circuits, but the general trend follows the plot shown.

In Figure 9, x=1 is the linear case (Class A – operation) and the values above x=15 produce narrow pulses. Class A operation gives higher output power but is not optimized for phase noise. However at higher drive levels, the transistor is "ON" for shorter duration, thus less loading and better phase noise, but at the cost of lower power output.

If the transistor is overdriven at the base, the collector current folds back (dip) and the actual current gain falls to values of 1.4 in our case (From Figure 9).

For the uncompressed current gain $(Y_{21}/Y_{11}) \approx (C_2/C_1) \approx 270pF/10pF$, the circuit will actually oscillate but does not have acceptable phase noise (low value of x, n=28, where $n = (C_1/C_2) +1$).

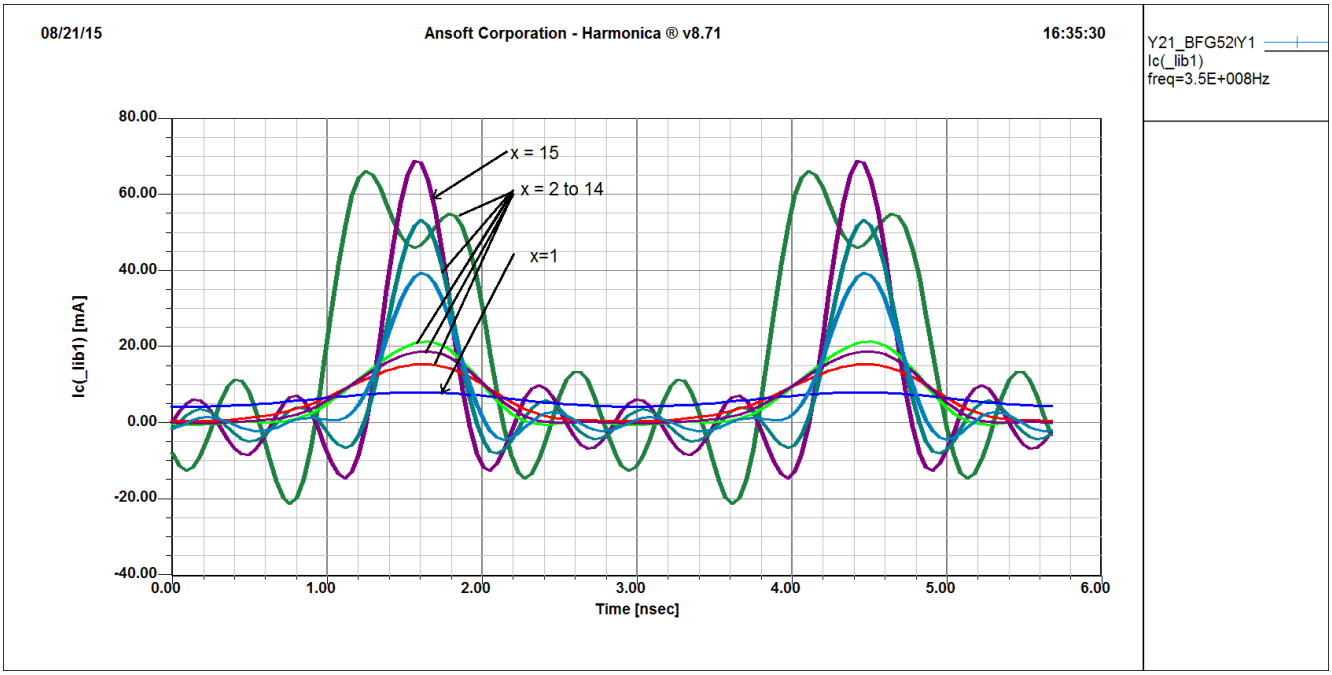

Figure 9: Shows I_c as a function of drive level. X

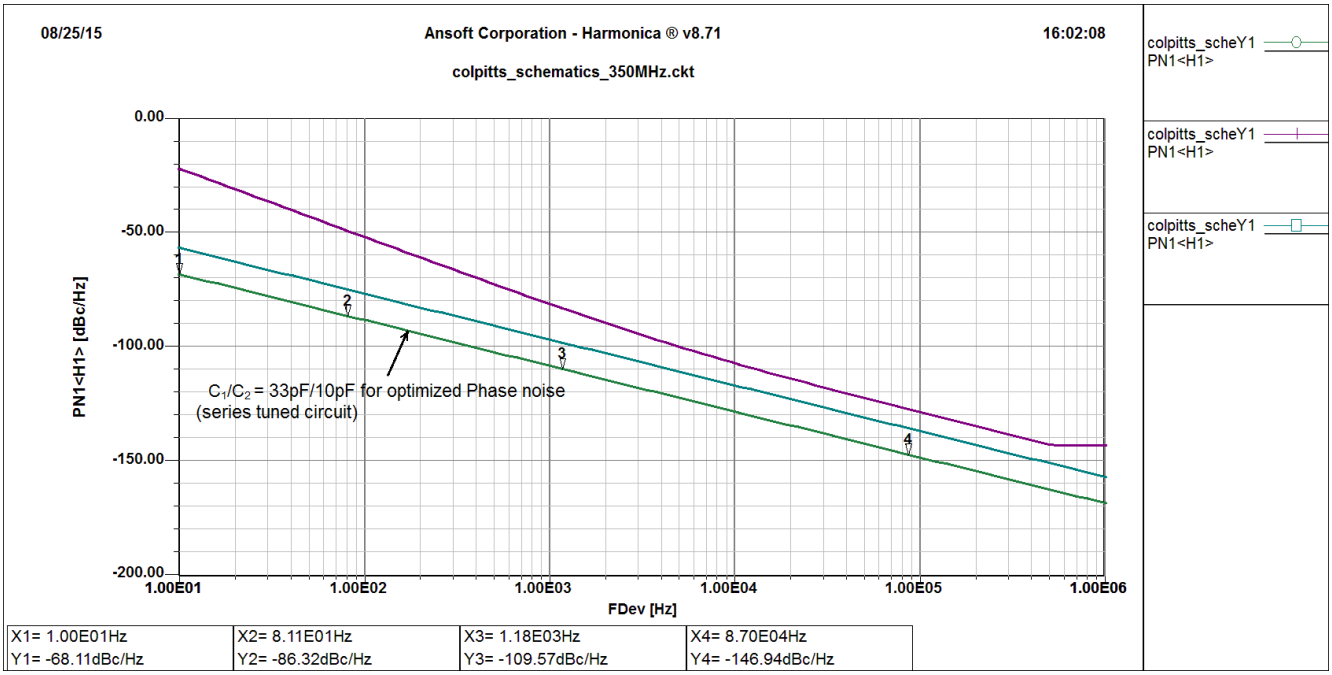

Figure 10: Optimization of Phase Noise for the series tuned circuit

By changing the capacitors C_1/C_2 to 33pF/10pF, n = 4.3, the phase noise performance is optimized, as shown in Figure 10. This circuit is a series tuned oscillator and now we move on to a high Q (from

Q=220 to Q=450) circuit, where the resonator is loosely coupled to the transistor. The tuned circuit consists of a 22nH inductor and 8.2pF capacitor. The following shows the design calculation for the parallel tuned circuit as found in ceramic resonator based oscillators.

The quality factor of the inductor is assumed 60 at 350 MHz, a low Q case.

The value of inductor is obtained as

$$Q_T = \frac{R_P}{\omega_0 L} \Rightarrow L = \frac{3649}{60 \times \omega_0} \qquad \text{(where } R_p \text{ is calculated using } \; G_m(x) = \frac{1}{R_P}\frac{C_1}{C_2}\left[1+\frac{C_2}{C_1}\right]^2 \tag{57}$$

$$L = \frac{3649}{60 \times 2\pi \times 350 \times E6} \approx 27nH \tag{58}$$

$$\omega = \sqrt{\frac{1}{L}\left[\frac{1}{C_1}+\frac{1}{C_2}\right]} \tag{59}$$

$$\omega^2 = \frac{1}{L}\left[\frac{1}{C_1}+\frac{1}{C_2}\right] = \frac{C_1 + C_2}{LC_1C_2} \tag{60}$$

The value of the capacitor is determined as

$$C_2 = \frac{2.55}{\omega^2 \times 17E - 9} \approx 14pF \tag{61}$$

$$C_1 \approx C_2 \approx 14pF \tag{62}$$

Taking into consideration the actual parasitics and RF parameters of the transistor, the optimized values are C_1 =12pF and C_2 = 8.2pF

Step 4: Calculation of the coupling capacitor C_c: [5, eqn (C-23)]

The expression for the coupling capacitor is

$$\frac{C}{10} > C_C > \left\{\frac{(\omega^2 C_1 C_2)(1+\omega^2 Y_{21}^2 L_P^2)}{[Y_{21}^2 C_2 - \omega^2 C_1 C_2)(1+\omega^2 Y_{21}^2 L_P^2)(C_1 + C_P + C_2)]}\right\} \tag{63}$$

C_c = 3.3pF (64)

Step 5: Calculation of the Phase Noise of the Colpitts Oscillator:

The mathematical expression of the phase noise of a Colpitts Oscillator is [5, pp180].

$$L(\omega) = 10Log\left\{\left[4kTR + \left[\frac{4qI_c g_m^2 + \frac{K_f I_b^{AF}}{\omega} g_m^2}{\omega_0^2 C_1^2 (\omega_0^2 (\beta^+)^2 C_2^2 + g_m^2 \frac{C_2^2}{C_1^2})}\right]\right]\left[\frac{\omega_0^2}{4\omega^2 V_{cc}^2}\right]\left[\frac{1}{Q^2} + \frac{[C_1 + C_2]^2}{C_1^2 C_2^2 \omega_0^4 L^2}\right]\right\} \quad (65)$$

where

$$\beta^+ = \left[\frac{Y_{21}^+}{Y_{11}^+}\right]\left[\frac{C_1}{C_2}\right]^p$$

$g_m = \left[Y_{21}^+\right]\left[\frac{C_1}{C_2}\right]^q$; values of *p* and *q* depends upon the drive level (x)

Y_{21}^+, Y_{11}^+ = large signal [Y] parameter of the active device

K_f = flicker noise coefficient

AF = flicker noise exponent

£(ω) = ratio of sideband power in a 1Hz BW at ω to total power in dB

ω = frequency offset from the carrier

ω_0 = center frequency

Q_L = loaded *Q* of the tuned circuit

Q_O = unloaded *Q* of the tuned circuit

kT = 4.1×10^{-21} at 300 K (room temperature)

R = equivalent loss resistance of the tuned resonator circuit

I_c = RF collector current

I_b = RF base current

V_{cc} = RF collector voltage

C_1, C_2 = feedback capacitor

Using a Mathcad calculation, we obtain the following results as shown in Figure 11, [5, eqn 8-109], which compares well with the measured data.

Phase Noise Equation

$Ic := 6.2 \cdot 10^{-3}$ $Ib := 43.2 \cdot 10^{-6}$ $L := 22 \cdot 10^{-9}$ $C_1 := 12 \cdot 10^{-12}$ $C_2 := 8.2 \cdot 10^{-12}$ $C_c := 3.3 \cdot 10^{-12}$

$K := 1.3806 \cdot 10^{-23}$ $T := 300$ $KT := 4.143 \cdot 10^{-21}$ $R := 0.3$ $Kf := 1 \cdot 10^{-7}$ $AF := 2$

$Q := 60$ $Vcc := 12$ $f := 350 \cdot 10^{6}$ $w0 := 2 \cdot \pi \cdot f$ $\beta := 140$

$r_e := \frac{26 \cdot 10^{-3}}{Ic}$ $gm1 := \frac{1}{r_e}$ $gm1 = 0.238$ $q := 1.602 \cdot 10^{-19}$ $i := 0..7$ $fo_i := 10^i$

wo_i is the frequecny offset from the carrier $wo_i := 2 \cdot \pi \cdot fo_i$

$$Lw_i := 10 \cdot \log\left[\left[4 \cdot KT \cdot R + \left[\frac{4 \cdot q \cdot Ic \cdot gm1^2 + \frac{Kf \cdot Ib^{AF}}{wo_i} \cdot gm1^2}{(w0)^2 \cdot C_1^2 \cdot \left[(w0)^2 \cdot \beta^2 \cdot C_2^2 + gm1^2 \cdot \frac{C_2^2}{C_1^2}\right]}\right]\right] \cdot \left[\frac{w0^2}{4 \cdot (wo_i)^2 \cdot Vcc^2} \cdot \left[\frac{1}{Q^2} + \frac{(C_1 + C_2)^2}{C_1^2 \cdot C_2^2 \cdot (w0)^4 \cdot L^2}\right]\right]\right]$$

fo_i	Lw_i
1	-5.227
10	-35.222
100	-65.165
$1 \cdot 10^3$	-94.633
$1 \cdot 10^4$	-121.303
$1 \cdot 10^5$	-143.272
$1 \cdot 10^6$	-163.529
$1 \cdot 10^7$	-183.555

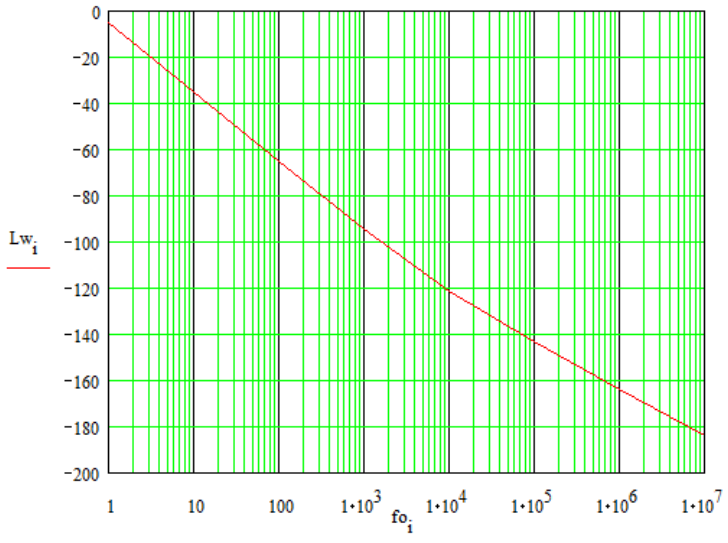

Figure 11: Mathcad calculation for phase noise

Measured results for a 350MHz Oscillator:

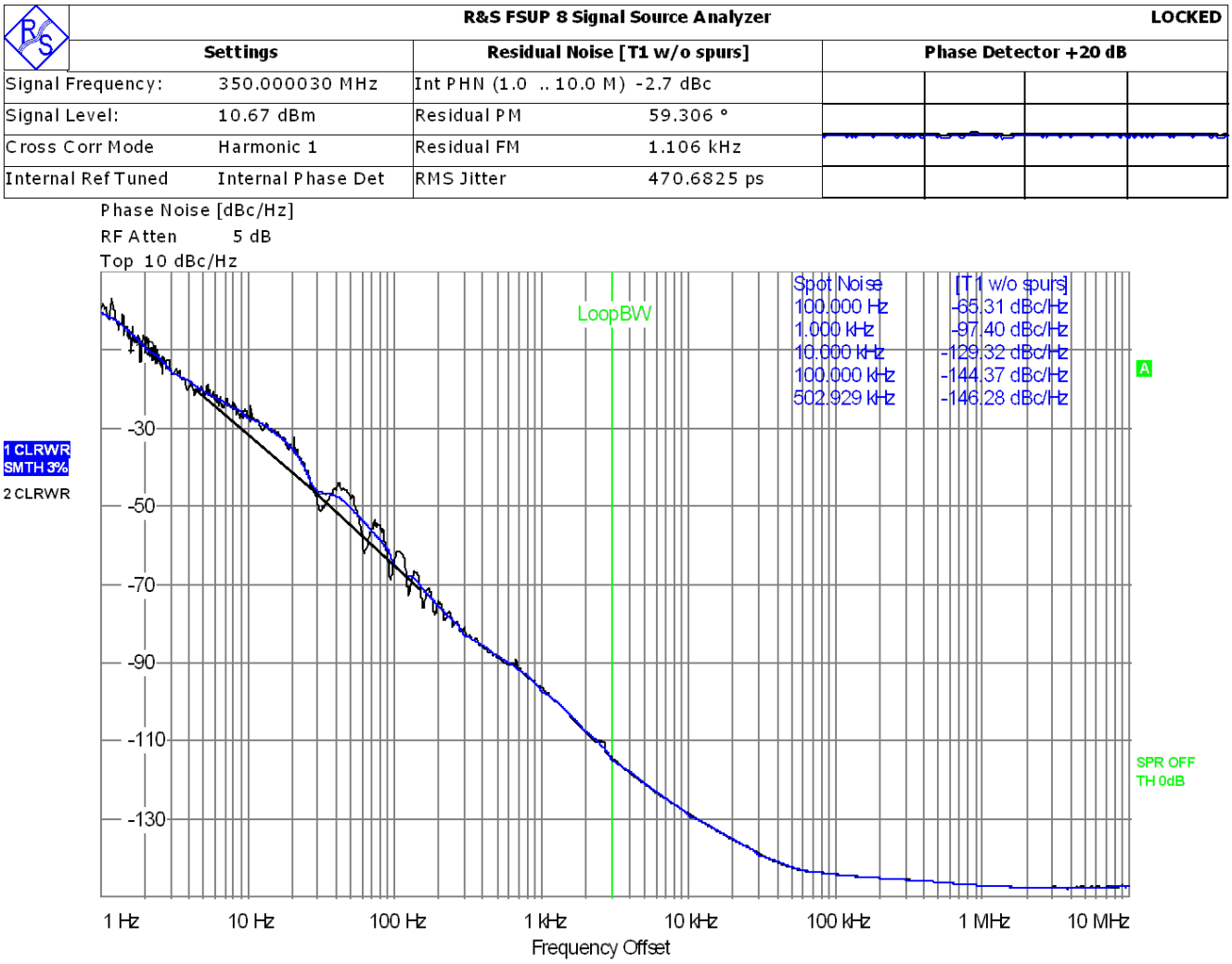

Figure 12: Measured Phase noise result for 350MHz Oscillator

The measured phase noise of the oscillator shown in Figure 12 is not quite comparable with the mathematics because it has a two stage buffer amplifier which isolates the oscillator from the output termination. This explains the limit of -146dBc/Hz at far-offset. At close-in, the phase noise is influenced by an AFC circuit. The real comparison should be done between 10Hz and 10 kHz offsets.

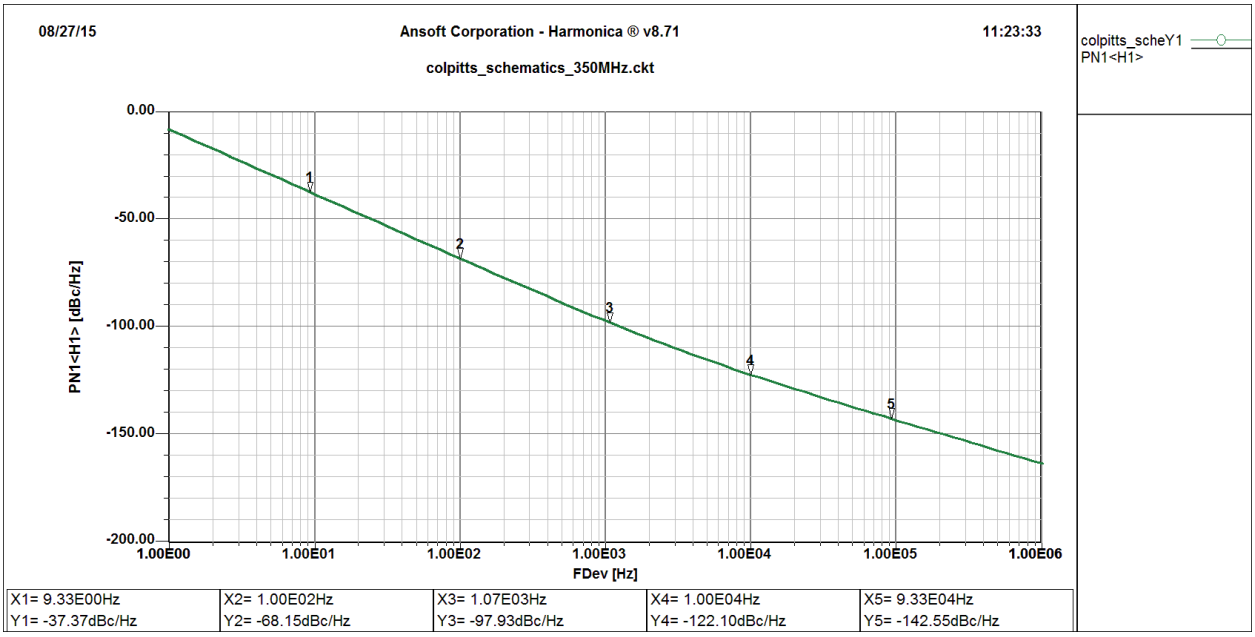

Figure 13a: Simulated Phase Noise for the 350MHz Parallel Tuned Colpitts configuration

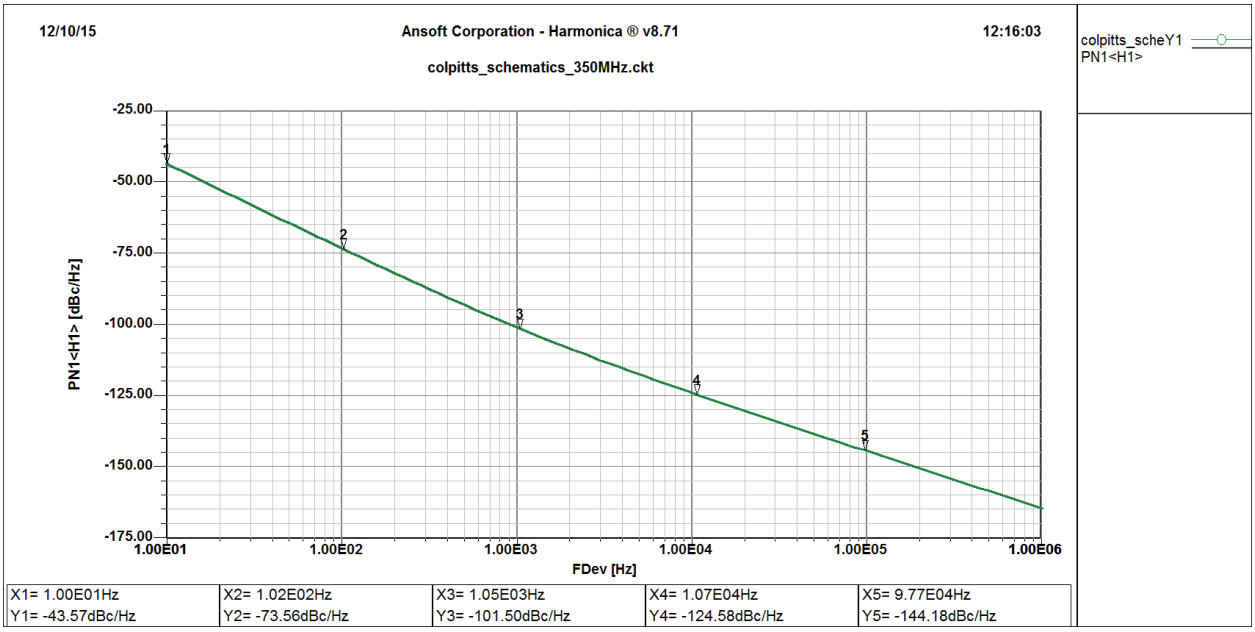

Figure 13b: Optimized - Simulated Phase Noise for the 350MHz Parallel Tuned Colpitts configuration

In order to optimize the phase noise for this type of oscillator,), using discrete components, the selection of the following set of values: C_p = 8.2pF, L=21nH, C_1=22pF, C_2=8.2pF, C_c=3.3pF improved the phase noise from -122dBc/Hz to -125dBc/Hz at 10 kHz offset. This is a result of trial-and-error, as

we do not know all the parasitics. Figure 13a shows the simulated phase noise plot and Figure 13b shows further improvement after optimizing the circuit for phase noise.

If we replace the parallel tuned circuit with a ceramic resonator (at this frequency range, Ɛr will be 88, the L/C ratio will be 0.048nH/pF vs. 2.44 nH/pF in case of discrete components used in our case), and the simulated phase noise is 105dBc/Hz at 10 kHz offset.

Note: ***This is due to the fact that the characteristic impedance of a ceramic resonator is much lower, than the discrete case***. $Z_0 = 60\Omega \frac{1}{\sqrt{\varepsilon_r}} \ln \frac{D}{d}$ (Where D = outer diameter and d= inner diameter of the ceramic resonator [[12], pp 754]. The prediction agrees well with the measured phase noise [[12], Fig (5-37)].

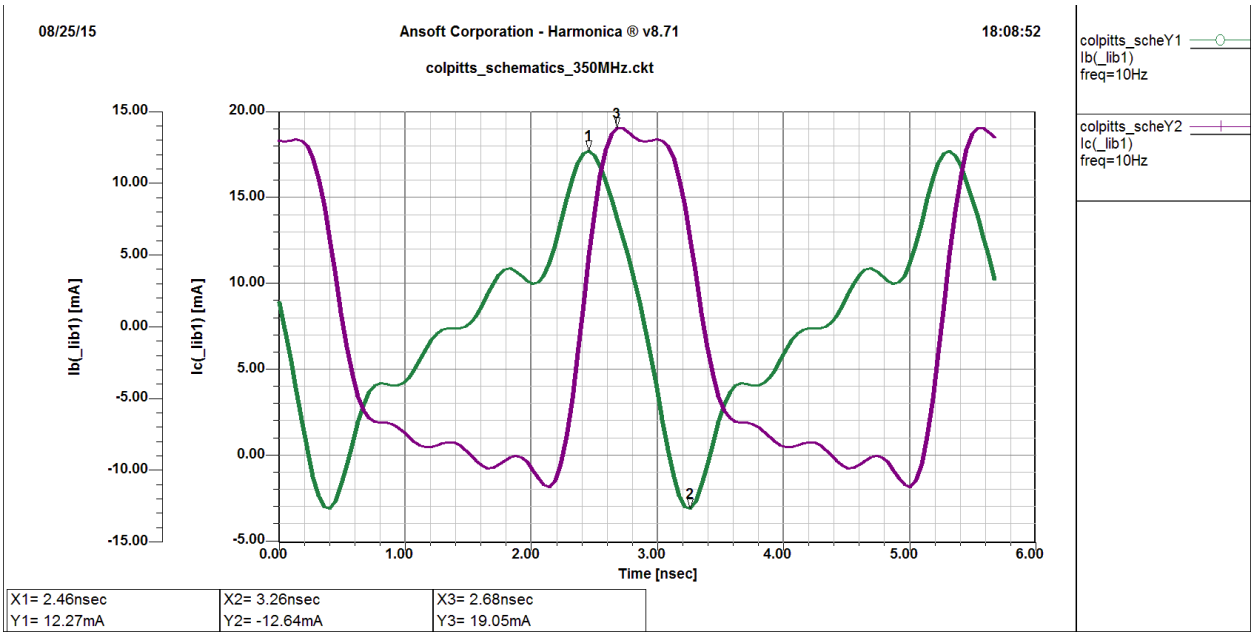

Figure 14: showing Y_{21}/Y_{11} large signal condition

Figure 14 shows the plots of the collector and base currents I_c and I_b for the optimized case (C_p=8.2pF, L=21nH (Q=60 at 350MHz), C_c=3.3pF, C_1=12pF, C_2=8.2pF).

From the plot in Figure 14, we can determine that the ratio of large signal $(Y_{21}/Y_{11}) = \beta = 1.4$. The next critical parameter, shown in Figure 15 is for the normalized drive level (x) is $V_1/(kT/q)$.

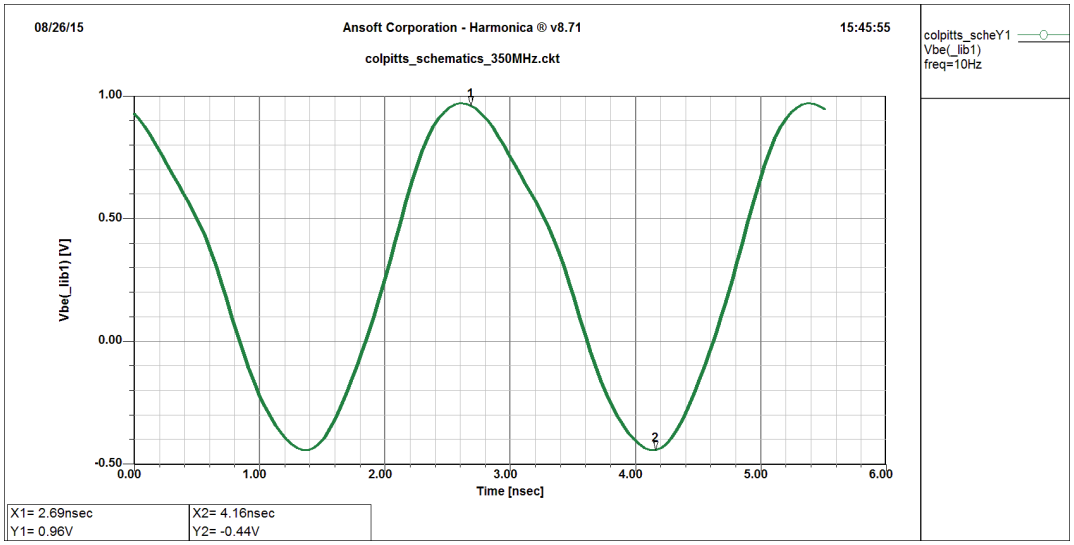

Figure 15: V_{be} – to calculate the drive level

From the Figure 15, the RMS value of V_{be} is used to determine the approximate drive level.

$$\text{Since } V_{be} = V_1, \text{ drive level (x)} \approx \frac{500\, mV_{rms}}{26\, mV} \approx 20 \qquad (66)$$

A table of normalized transconductance as a function of the drive level including the large values is given in Table 2 [5].

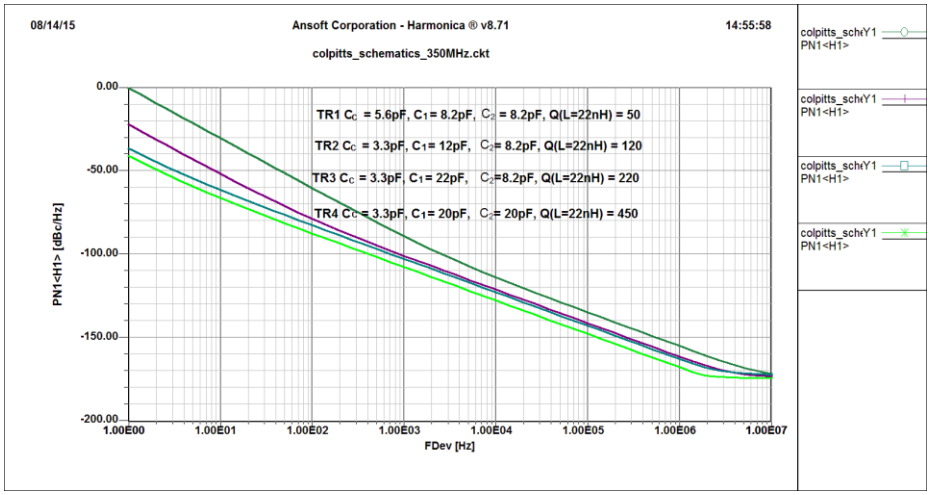

Figure 16: Optimized phase noise for different values of Inductor Q

Figures 16 and 17, show the phase noise variation with variation in Q (L=22nH) in the LC resonator. The output power, collector current, and base voltage (V_b) and (V_{be}) plots are also shown for the same combination.

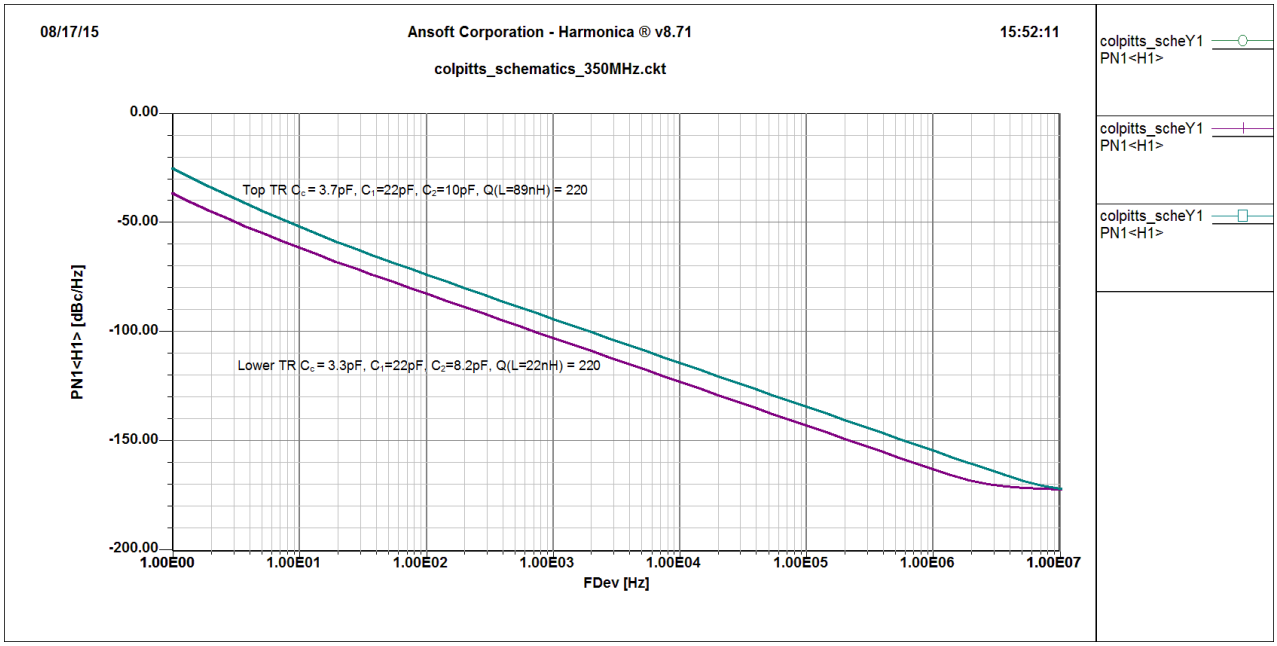

Figure 17: Results of Series and Parallel tuned circuits for same value of Inductor Q

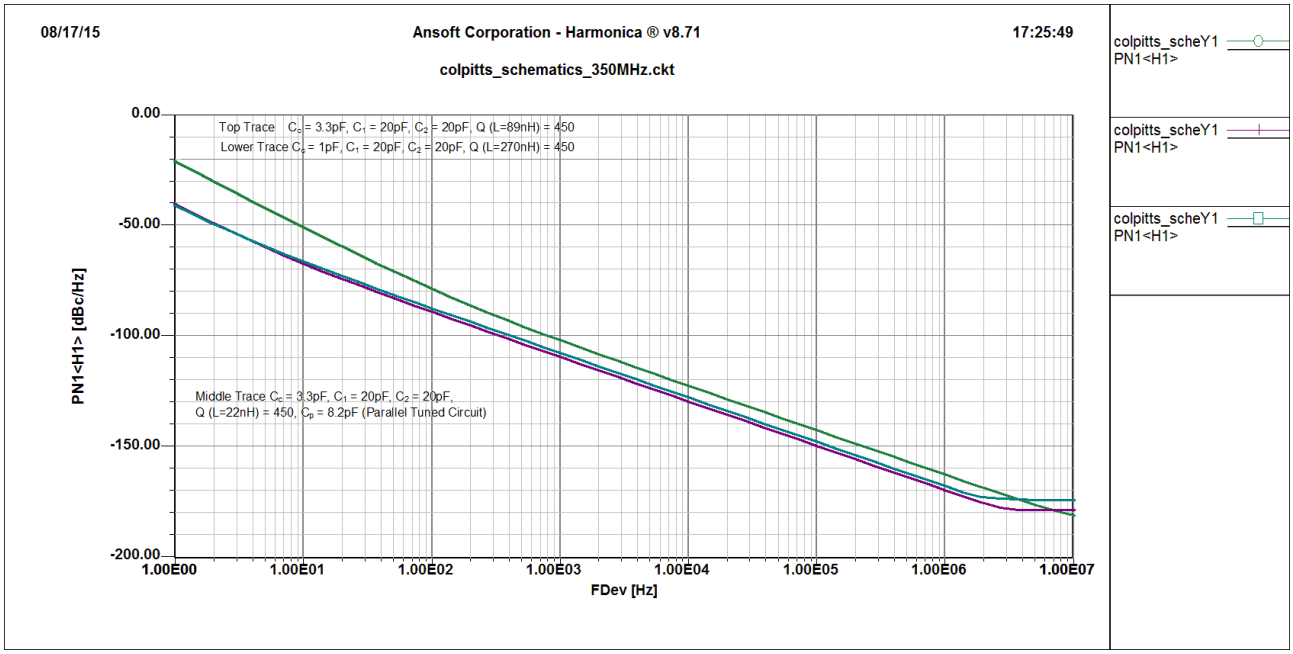

Figure 18: Results of Series and Parallel tuned circuits for higher value of Inductor Q

The parallel tuned circuit shows better phase noise performance, as seen in Figure 18, due to the fact that the rate of change of reactance in a parallel tuned circuit is significantly larger than in a simple series tuned oscillator.

1/f Noise:

The electrical properties of surfaces or boundary layers are influenced energetically by states, which are subject to statistical fluctuations and therefore, lead to the flicker noise or 1/*f* noise for the current flow.

1/*f* - noise is observable at low frequencies and generally decreases with increasing frequency *f* according to the 1/*f* - law until it will be covered by frequency independent mechanism, like thermal noise or shot noise.

Example: The noise for a conducting diode is bias dependent and is expressed in terms of AF and KF.

$$\langle i_{Dn}^2 \rangle_{AC} = 2qI_{dc}B + KF\frac{I_{DC}^{AF}}{f}B$$

- The AF is generally in range of 1 to 3 (dimensionless quantity) and is a bias dependent curve fitting term, typically 2.
- The KF value is ranging from 10^{-12} to 10^{-6}, and defines the flicker corner frequency. [32]

One of the important characteristics for device evaluation and selection is 1/f noise, which is a function of the active device characteristics and a major contributor to phase noise, especially in applications such as VCOs [5, 20]. In an oscillator, 1/f noise that is present in transistors at low frequencies is upconverted and added to the phase noise around the carrier signal. Hence, proper characterization of 1/f noise and its effects on phase noise is an important topic. In addition, 1/f noise is not solely an active device phenomenon. Passive devices such as carbon resistors, quartz resonators, SAW devices, and ceramic capacitors are among devices that show presence of this phenomenon when used as part of

low-noise electronic systems. Generally, 1/f noise is present in most physical systems and many electronic components [19, 22, 23].

Flicker noise in BJTs is also known as 1/f noise because of the 1/f slope characteristics of the noise spectra. This noise is caused mainly by traps associated with contamination and crystal defects in the emitter-base depletion layer. These traps capture and release carriers in a random fashion. The time constants associated with the process produce a noise signal at low frequencies. The flicker noise spectral density is given by:

$$S(f)df = (KF)IB^{AF}df/Fc \tag{67}$$

where:

KF = flicker noise constant

AF = flicker noise exponent

IB = DC base current

Fc = flicker noise corner frequency

The measured flicker corner frequency, F_{meas}, is determined by noting the intersection of the 1/f noise spectrum and the white noise spectrum. This intersection is where the measured flicker noise power and the white noise power are equal. To determine F_{bn}, the intrinsic base flicker noise corner, requires solving the following equation [20, 21]:

$$F_{bn} = F_{meas}\,[1 + 1/\beta + 2V_{th}G_{in}/IB] \tag{68}$$

where:

F_{bn} = intrinsic base flicker noise corner

F_{meas} = measured flicker corner

β = collector-base current gain

V_{th} = thermal voltage = kT/q

G_{in} = external input conductance

IB = DC base biasing current

The equation for the intrinsic base flicker corner modifies the measured flicker corner to account for the input conductance, base current, and DC current gain of the device. The formula for F_{bn} is valid provided the measured output noise characteristics are dominated by the base flicker and base shot noise sources.

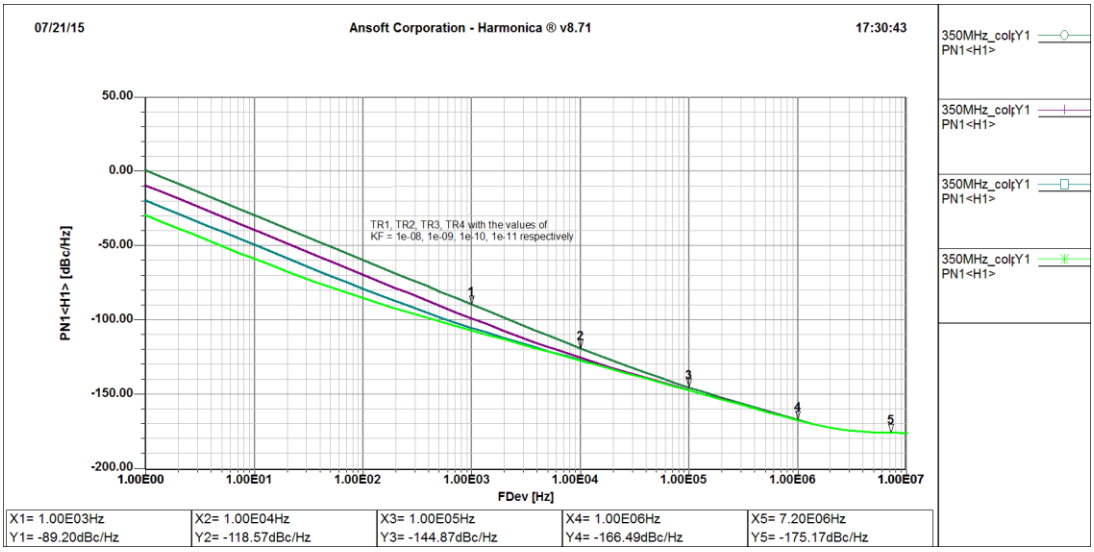

Figure 19: Effect of KF factor on Phase Noise

Changing the KF and AF factors, affects the phase noise as can be seen from the plots.

Y-intercept of the 1/f spectra increases proportionally to KF, which is in accordance with equation (34). The Y-intercept of the 1/f spectra decreases more rapidly with increase in AF. The following discussion of the tuning diodes results in a noise contribution similar to this flicker mechanism.

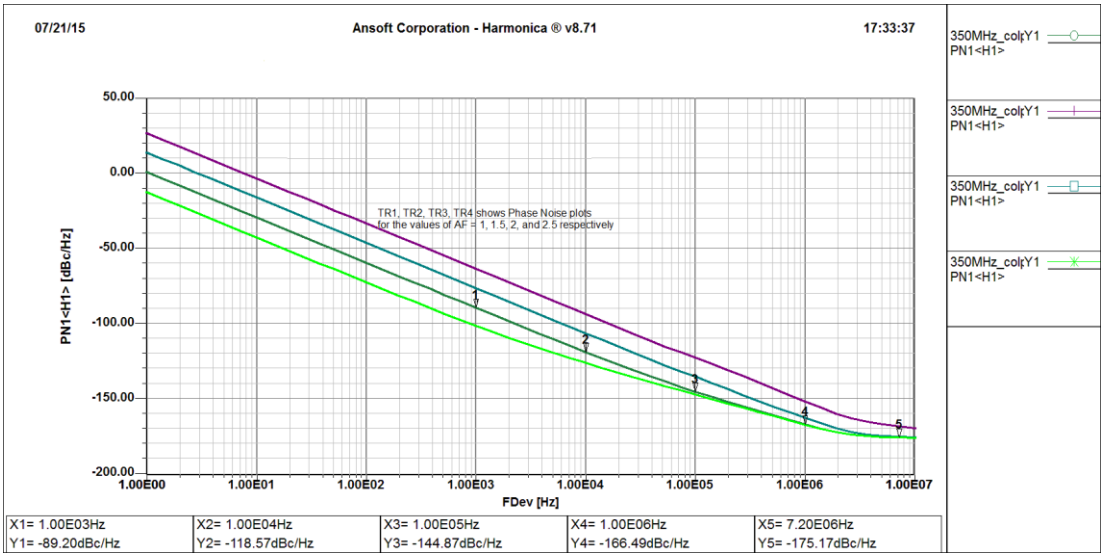

Figure 20: Effect of AF factor on Phase Noise

AM-to-PM Conversion from tuning diodes

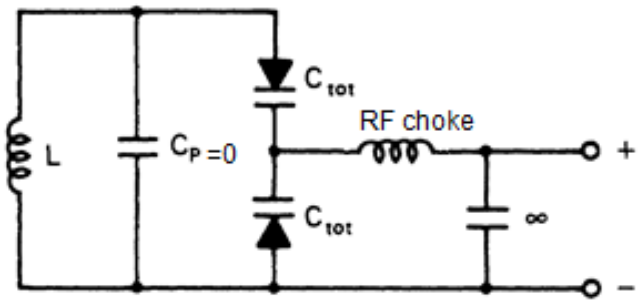

Figure 21: Parallel tuned circuit with tuning diodes

Figure 21 shows a parallel tuned circuit which is connected to the oscillator discussed above. The frequency change is obtained by applying a positive voltage to the + terminal. The parallel capacitor is replaced by the two tuning diodes. Here we will show the influence of the tuning diodes in the voltage-controlled oscillators, the resulting phase noise generated by tuning diodes is shown in Figure 22.

It is possible to define an equivalent noise R_{aeq} that, inserted in Nyquist's Johnson noise equation,

$$V_n = \sqrt{4kT_o R\Delta f} \tag{69}$$

where kT_o=4.2 × 10^{-21} at about 300 K, R is the equivalent noise resistor, and Δf is the bandwidth, determines an open-circuit noise voltage across the tuning diode. Practical values of R_{aeq} for carefully selected tuning diodes are in the vicinity of 200 Ω to 50 kΩ. If we now determine the noise voltage, $V_n = \sqrt{4 \times 4.2 \times 10^{-21} \times 10{,}000}$ the resulting voltage value is $1.296 \times 10^{-8}\ \mathrm{V}\sqrt{\mathrm{Hz}}$.

This noise voltage generated from the tuning diode is now multiplied with the VCO gain K_o, resulting in the rms frequency deviation

$$\left(\Delta f_{\mathrm{rms}}\right) = K_o \times \left(1.296 \times 10^{-8}\ \mathrm{V}\right) \text{ in 1-Hz bandwidth} \tag{70}$$

To translate this into an equivalent peak phase deviation,

$$\theta_d = \frac{K_o\sqrt{2}}{f_m}\left(1.296 \times 10^{-8}\right) \text{ rad in 1-Hz bandwidth} \tag{71}$$

or for a typical oscillator gain of 100 kHz/V,

$$\theta_d = \frac{0.00183}{f_m} \text{ rad in 1-Hz bandwidth} \tag{72}$$

For f_m = 25 kHz (typical spacing for adjacent-channel measurements for FM mobile radios), the θ_c = 7.32 × 10^{-8}. This can be converted now into the SSB signal-to-noise ratio:

$$\mathcal{L}(f_m) = 20\log_{10}\frac{\theta_c}{2} = -149\ \mathrm{dBc/Hz} \tag{73}$$

For the typical oscillator gain of 10 MHz/V found in wireless applications, the resulting phase noise will be 20 dB worse [10 log (10 MHz ÷ 100 kHz)]. However, the best tuning diodes, like the BB104, have an R_n of 200 Ω instead of 10 kΩ, which again changes the picture. Therefore, with kT_o = 4.2 × 10^{-21} the resulting noise voltage will be

$$V_n = \sqrt{4 \times 4.2 \times 10^{-21} \times 200} = 1.833 \times 10^{-9}\ \mathrm{V}\sqrt{\mathrm{Hz}} \tag{74}$$

From (72), the equivalent peak phase deviation for a gain of 10 MHz/V in a 1-Hz bandwidth is then

$$\theta_d = \frac{1\times10^7\sqrt{2}}{f_m}\left(1.833\times10^{-9}\right) \text{ rad} \tag{75}$$

or

$$\theta_d = \frac{0.026}{f_m} \text{ rad in 1 - Hz bandwidth} \tag{76}$$

With f_m = 25 kHz, $\theta_c = 1.04 \times 10^{-6}$. Expressing this as phase noise:

$$\mathcal{L}(f_m) = 20\log_{10}\frac{\theta_c}{2} = -126 \text{ dBc/Hz} \tag{77}$$

Figure 22 shows the influence of the tuning diode on the phase noise. For the purpose of discussion, the equivalent noise resistance is assumed 1kΩ, and 3 sensitivity curves are shown. For a tuning sensitivity of more than 100 kHz/V the varactor noise dominates. As the tuning sensitivity increases the influence of the oscillator noise itself disappears.

Summary:

With a systematic approach to the Colpitts oscillator this paper provides information for an optimized design and the resulting phase noise. Starting with the explanation about the Colpitts oscillator, invented in 1918, we have discussed a linear analysis based on Y-parameters, followed by S-parameter approach, which is applicable to practically all oscillators and then move into the important time-domain analysis. This allows a very reliable design, where the simulated, calculated and the measured results agree well. This detailed analysis gives a thorough insight into the design approach and results of a Colpitts oscillator. Finally the noise contribution of the tuning diodes is added. The interested reader, having access to CAD tools can run some "experiments" by varying the component values.

At this point we would also like to thank our reviewers for their valuable suggestions to optimize this paper.

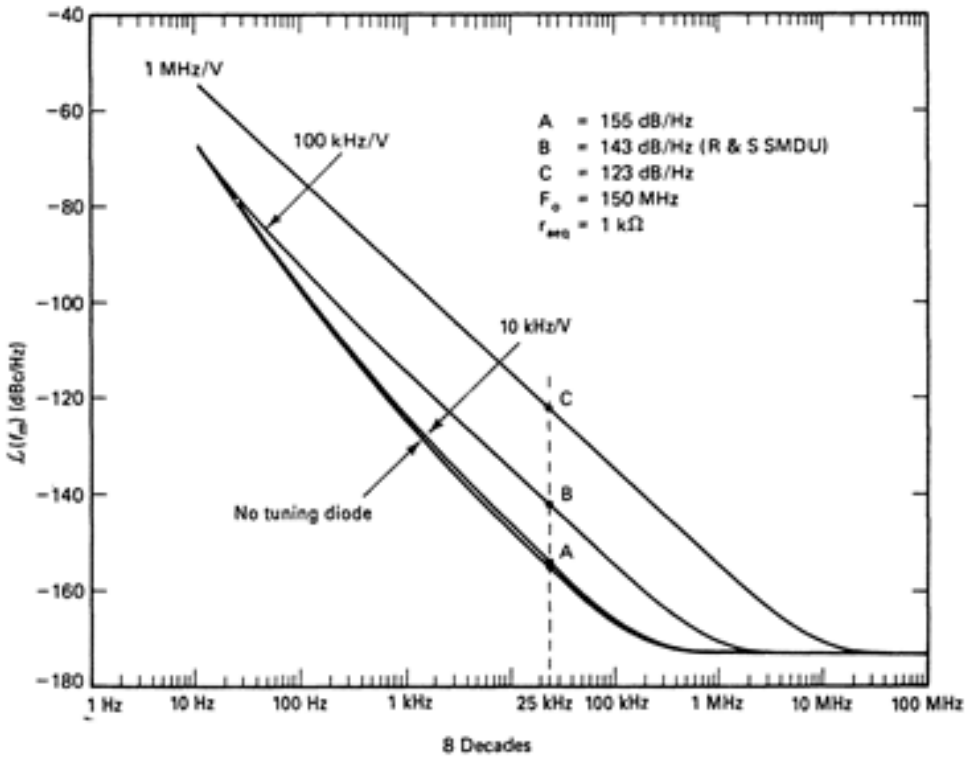

Figure 22: Influence of tuning diode on phase noise

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