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QST Issue: May 2005
Title: Hands-On Radio: Experiment #28: The Common Base Amplifier
Author: H. Ward Silver, N0AX

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Experiment #28: The Common Base Amplifier

Even though it looks "funny," the common base amplifier and the FET common gate amplifier perform some pretty useful tricks. They're more common than you think!

Terms to Learn

- *Indirect Measurement*—calculating the value of a parameter from the measured values of other parameters
- *Isolation*—a lack of effects on one circuit from changes in another circuit
- *Self-biased*—a circuit that operates at a fixed bias point without a separate biasing circuit

Introduction

Common-base (CB) and common-gate (CG) amplifiers are the third form of single-transistor amplifier circuit topology. Their claim to fame is low input impedance, high voltage gain and high output resistance. This makes them a good choice for RF amplifiers. You may have already made use of the vacuum tube version of the CB circuit—a grounded-grid amplifier! As we discuss these amplifiers, I'll make reference to previous experiments that can be downloaded from the Hands-On Radio Web site, **www.arrl.org/tis/info/HTML/Hands-On-Radio/**.

CB and CG Circuits

Figure 1 shows the CB amplifier—the transistor is turned on its side, with the emitter facing the input. How can that possibly amplify anything? Understanding, as it often does, comes from changing one's view of a problem. Figure 1 redraws the odd-looking regular CB circuit in the more familiar common-emitter style. The input is just moved from the base circuit to the emitter circuit.

Remember—the input signal only needs to cause changes in the transistor base-emitter current. Placing the input in the emitter circuit does exactly that, except that a positive change in input amplitude *reduces* base current by lowering V_{BE}, thus raising V_C. As a result, the CB amplifier is *non-inverting* with output and input signals in-phase.

Practical circuits for the CB and the JFET CG circuit are shown in Figure 2. Looking at the CB amplifier from a dc point of view (replace the capacitors with open circuits), all of the same resistors are there as in the good old common-emitter amplifier we learned about in Experiment #1. The input capacitors, C_{IN}, allow the dc emitter (or source) current to flow "around" the ac input signal source.

Let's analyze the CB amplifier first. Since the input signal is also the ac emitter current, i_e, the ac collector current must be:

$$i_c = i_e\,[\beta/(\beta+1)] \text{ so, current gain } A_I = i_c/i_e = [\beta/(b+1)] \qquad [1]$$

Current gain is always just below unity, just as voltage gain for the EF amp is just below unity. The neat thing about the CB amplifier is that you can hang just about any load resistance on the output and current gain is unchanged. This configuration has excellent *isolation* between output and input, meaning changes in load don't affect the input impedance—a good thing for RF systems that require stable impedances.

By making the load resistance greater than the input resistance while keeping current constant, you get voltage gain. To calculate the input resistance of the CB amp, we encounter a new transistor parameter, h_{ie}, representing the resistance between the base and emitter. Following reasoning similar to that for the emitter follower (EF) amplifier (see Experiment #2), explaining why current gain multiplied the effect of R_E at the input, we find that input resistance for the CB amp is:

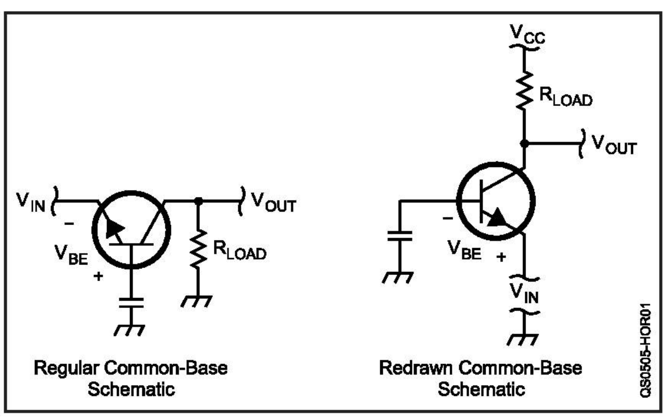

Figure 1—The Common Base amplifier can be redrawn to show its similarity to the better-known Common Emitter amplifier.

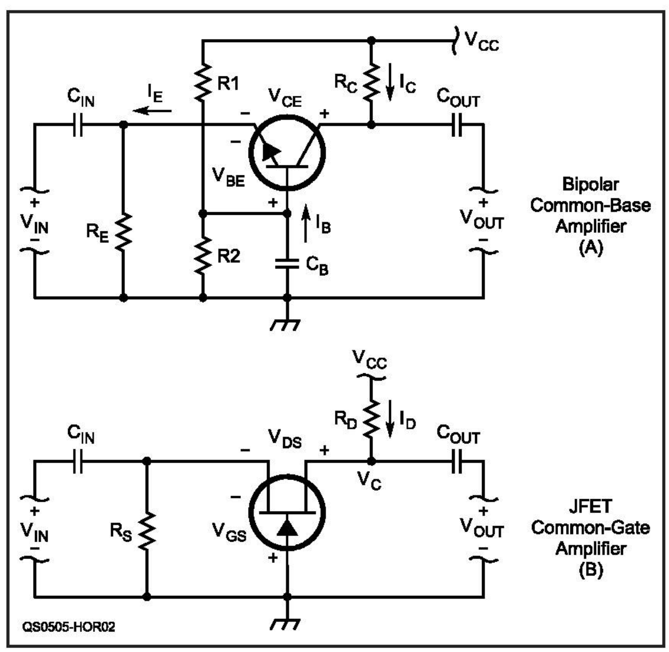

Figure 2—The Common Base and Common Gate amplifiers are great wide-bandwidth amplifiers, with low input impedance and good voltage gain.

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$R_{in} = h_{ie}/(1 + \beta)$ and $v_{in} = R_{in}\, i_e$ [2]

For a 2N3904 transistor, h_{ie} averages about 1 kΩ between 1 and 10 mA of collector current and β is about 150 over the same range. That means the input resistance will be about 6 Ω. A more sophisticated analysis will come up with a somewhat higher figure—around 20 Ω—but the CB input resistance is still quite low and can be controlled by changing the bias current. Transistors used as preamplifiers are designed with h_{ie} to result in a 50 Ω input resistance for reasonable values of collector current.

To figure voltage gain, A_V, start with $v_o = i_c\, R_L$ and make substitutions from equations 1 and 2. R_L is the parallel combination of R_C and whatever load is attached at V_{OUT}.

$A_V \approx \beta(R_L/h_{ie})$ [3]

It doesn't take a big load resistance to create a substantial voltage gain. Using the 2N3904 again, a 500 Ω load results in A_V = 150 (500/1000) = 75. This is why the CB and CG amplifiers are often used as preamplifiers.

Setting the operating or Q point of the CB amplifier starts with selecting A_V and calculating the required R_L—the parallel combination of R_C and whatever load is connected at V_{OUT}. Determine R_C and proceed to determine R_E, R_1 and R_2, as in the CE amplifier.

In the JFET common-gate amplifier circuit one of the bias resistors is missing. What's up with that? This is called a *source self-biased* circuit. For a depletion-mode JFET, V_{GS} needs to be somewhere between 0 V and V_P, the pinch-off voltage. One way to make V_{GS} negative would be to use a negative supply, but it's easiest to hold V_G at 0 V (by grounding it) and raise V_S instead. With V_G=0:

$V_{GS} = -I_{DS}R_S$ [4]

Since V_{GS} and I_{DS} are predetermined as the selected Q point, you can easily solve for R_S.

The JFET CG performance equations are:

$R_{IN} \approx 1/g_m$, where g_m is the JFET transconductance
$A_V = g_m R_D$

Input and Output Resistance

Much is made of the input and output resistances of the CB/CG amplifier. Can they be measured? Not directly, such as with a VOM, but indirectly, by adding external resistances and observing the effect on the circuit. These methods are illustrated in Figure 3.

Let's start with input resistance. When combined with an external resistor, R_{ADJ}, the amplifier's input resistance, R_{IN}, forms a voltage divider. If I know V_{IN} and V_E, and I can measure R_{ADJ}, I can calculate R_{IN}. Input a known voltage V_{IN} and adjust R_{ADJ} until V_E (measured across R_E) is $^1/_2 V_{IN}$. At this point, the resistances in the divider are equal, so $R_{IN} = R_{ADJ}$.

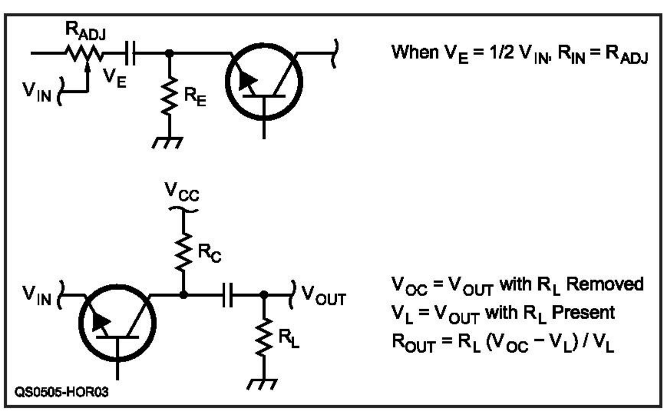

Figure 3—Input and output impedance of amplifier circuits must be measured indirectly.

Measuring output resistance is a two-step process. First, disconnect the load resistor, R_L, entirely, and measure the open-circuit voltage, V_{OC}. Then connect a load resistor between one-half and twice the expected value of R_{OUT}. Measure the output voltage, V_L. Once again, you have a voltage divider and, with a little math:

$R_{OUT} = R_L\,(V_{OC} - V_L) / V_L$ [5]

For most transistors in this circuit, R_{OUT} will be approximately the same as R_C. Ready to try it out? Let's go!

Building and Testing a CB Amplifier

In this experiment, you'll build a CB amplifier, measure the voltage gain, and then measure the input and output resistance. Start by constructing the amplifier circuit of Figure 2A using resistor values from Experiment #1 (R1 = 39 kΩ, R2 = 6.8 kΩ, R_C = 1.5 kΩ, R_E = 270 Ω), $C_{IN} = C_B = C_{OUT}$ = 10 µF (connect + leads to transistor) and V_{CC} = 12 V. Use equation 3 to calculate the expected value of A_V with R_C as the load. Assume that β=150 and h_{ie} = 1000 Ω. Use equation 2 to calculate the expected value of R_{IN}.

- Confirm that the circuit is operating at its Q point: $V_{CEQ} \approx 5$ V and $I_{CQ} \approx 4$ mA.
- Apply a 10 kHz sine wave to the input at a voltage small enough so that the output is not distorted. (You may have to use a voltmeter to accurately measure the voltage.) Measure the output voltage (which is V_{OC}) and calculate the gain. I obtained a gain of 150. Measured gain will be somewhat lower than the calculations because our equation is somewhat oversimplified. (Voltmeter users—confirm distortionless operation by making sure that changes in the input cause a proportional change in the output.)
- Measure input resistance by placing a 100 Ω potentiometer in series with the input signal and adjusting it until the ac value of $V_E = {}^1/_2\, V_{IN}$. Remove the potentiometer and measure its value—mine was 10.2 Ω.
- Reconnect the input signal directly to C_{IN}. Add a load resistor, R_L = 1 kΩ by connecting it from the OUTPUT side of C_{OUT} to ground, *not* from the collector to ground—that would change the dc biasing. Calculate R_{OUT} by using equation 5. R_{OUT} should be almost the same as R_C—mine was 1.59 kΩ.
- Experiment with different values of load resistance to see what happens to gain.

Shopping List

- 2N3904 transistor
- 270 Ω, 1 kΩ, 1.5 kΩ, 6.8 kΩ, 39 kΩ ¼ W resistors
- 3—10 µF electrolytic capacitors
- 100 Ω potentiometer

Suggested Reading

Common-base amplifiers are not often covered in detail, since they are not common. Chapter 6 of TAB Books' *Guide to Understanding Electricity and Electronics*, 2nd edition, has broad coverage of all three types of amplifier circuits. A simple UHF preamplifier project using a JFET is available at **www.dxzone.com/cgi-bin/dir/jump2.cgi?ID=9258**.

Next Month

Who is this Kirchhoff guy and what are his laws that electrical engineers keep referring to? Tune in next month and learn about two fundamentals of all circuit analysis and design—Kirchhoff's Voltage and Current Laws. QST

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QST Issue: Feb 2003
Title: Hands-On Radio: Experiment #1--The Common-Emitter Amplifier
Author: H. Ward Silver, N0AX

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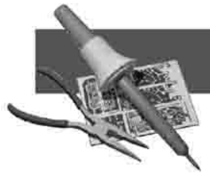

Experiment #1—The Common-Emitter Amplifier

Our first experiment will feature the *common emitter* (CE) *amplifier*. Why the CE amplifier? It is the most common amplifier configuration of all—it is found in analog and digital circuits, from dc through microwaves and it is made of discrete components and fabricated in integrated circuits (ICs). If you understand the CE amplifier, you've made a good start in electronics.

Background

The CE amplifier (Figure 1) is used when modest voltage gain is required along with an input impedance (the impedance seen by the circuit supplying the signal to be amplified) of a few kΩ or more. The output of the CE amplifier is inverted from its input. (We call this 180° of phase shift.) As the input signal swings positive, more current flows into the transistor's base, which also causes more current to flow from the collector to the emitter. This causes more voltage drop across Rc and so the voltage at the collector also drops. The reverse is true when the input signal swings negative.

In order for the circuit to amplify both positive and negative swings of the input signal, its collector current (I_c) must be offset from zero so that it can both increase and decrease. An amplifier that has a continuous output current, even with no input signal, is called a Class A amplifier. The method of controlling this continuous current is called biasing. Resistors in the voltage divider R1 and R2 cause a small amount bias current to flow into the base and thus keep the collector current flowing at all times. The amplifier is then said to be operating in its "active" region. The resulting continuous collector current equals the base bias current multiplied by the transistor's current gain, β. Using Ohm's Law to find the voltages across R_c and R_e, the transistor's collector-to-emitter voltage (V_{ce}) is also determined by the bias current. The combination of continuous I_c and V_{ce} is called the Q-point of the circuit, where Q stands for "quiescent." When an input signal is applied, output voltage and current changes are centered around the Q-point.

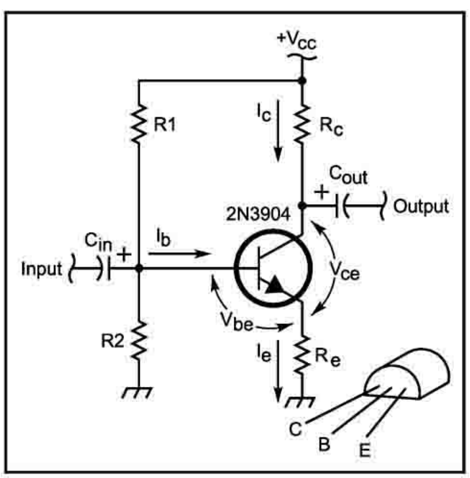

Figure 1—The common-emitter amplifier.

As the collector current changes in response to an input signal, the circuit's output voltage is developed across the collector resistor, R_c. For a given input signal, a larger R_c means a larger output voltage change—a higher voltage gain (A_v). The function of R_e is to set the transistor's Q-point such that the collector voltage can make wide swings without running up to the power supply voltage (V_{cc}) or down to ground. By being in the collector current's path, along with R_c, larger values of R_e work against R_c to reduce voltage gain. In fact, the voltage gain is approximately the ratio of R_c to R_e.

Figure 1 shows capacitors at the input (C_{in}) and output (C_{out}). This is called an "ac coupled" design. The capacitors block the flow of dc current to the load or to the circuit driving the amplifier. These capacitors also cause the gain at very low frequencies to be reduced, as the impedance of a capacitor increases at low frequencies—hence the gain at dc is zero. For this experiment, all capacitors will be 10 µF—a value large enough to act as a short-circuit for most audio signals. If polarized capacitors are used, the positive side should be connected to the circuit.

Terms to Learn

A_v—Voltage gain, the ratio of output to input voltage.

Beta (β)—DC current gain, the ratio of collector current to base current.

Cutoff—Collector current reduced to zero.

I_b, I_c—Base and collector current, respectively.

Q-Point—Quiescent or resting values of collector current (I_{cq}) and voltage (V_{ceq}) with no applied input signal.

V_{ce}, V_{be}—Voltage from collector-to-emitter and base-to-emitter, respectively.

Key Equations

$$I_c \approx I_e,\ I_c = I_b \times \text{Beta}\ (\beta) \quad [1]$$

$$V_{cc} = (I_c \times R_c) + V_{ce} + (I_e \times R_e) \approx I_c \times (R_c + R_e) + V_{cc} \quad [2]$$

$$A_v \approx R_c / R_e \quad [3]$$

$$V_{R2} = V_{be} + (I_e \times R_e) \quad [4]$$

Designing the Amplifier

1. Choose the circuit's operating requirements:

V_{cc} = 12 V *(our power supply voltage).*

A_v = 5 *(a medium value of gain).*

Q-point of I_{cc} = 4 mA *(a value to keep power dissipation low)* and V_{ceq} = 5 V *(rule of thumb—about one-half of V_{cc}).*

Assume the transistor's β is 150 and base-to-emitter voltage, V_{be} = 0.7 V. *(The actual range of β can be read from the transistor's data sheet and V_{be} is typically 0.7 V for silicon transistors.)*

2. *From equation 2,* $V_{cc} = I_c (R_c + R_e) + V_{ce}$

$(V_{cc} - V_{ce}) / I_c = R_c + R_e$, so $R_c + R_e = (12\ \text{V} - 5\ \text{V}) / 4\ \text{mA} = 1.75\ \text{k}\Omega$

3. *From the above,* $R_c = 1750\ \Omega - R_e$ and with $A_v = 5$, $R_c / R_e = 5$ *(equation 3)* so

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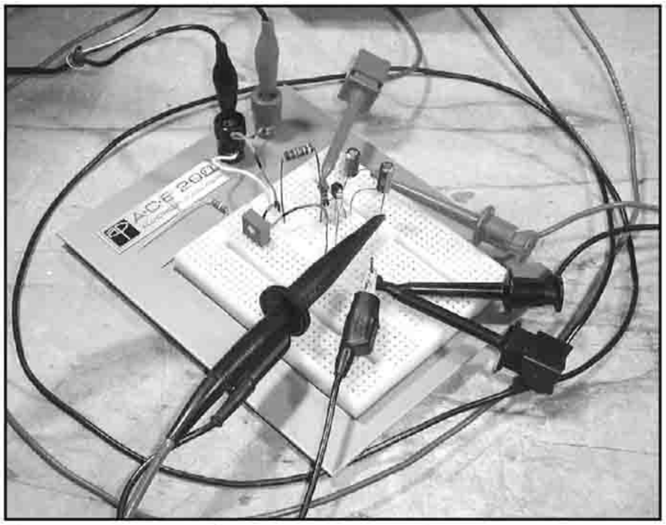

Figure 2—The experimental setup, showing the prototype board and connections to the power supply, oscilloscope and voltmeter. Note that the signal instrument grounds are all connected to a single point—this helps to prevent noise pickup and ground loops.

R_c = 5 R_e and (1750 Ω – R_e) = 5 R_e, so 6 R_e = 1750 Ω and R_e = 1750 Ω / 6 = 292 Ω *(use 270 Ω, a standard value).*

4. *From equation 1,* base current, $I_b = I_{cq} / \beta$ = 4 mA / 150 = 26.67 µA (27 µA). Set the current through R1 and R2 equal to 10 times I_b or 270 µA. *(This is a rule of thumb simplifying calculations and keeping I_b stable with a "stiff" bias supply.)*

The voltage across R2 = V_{be} + I_c (R_e) = 0.7 V + 4 mA (270 Ω) = 1.8 V *($I_c \approx I_e$ and equation 4).*

By Ohm's Law, R2 = 1.8 V / 270 µA = 6.7 kΩ *(use 6.8 kΩ, a standard value).*

The voltage across R1 = V_{cc} – 1.8 V = 10.2 V *(voltage divider)*

By Ohm's Law, R1 = 10.2 V / 270 µA = 37.8 kΩ *(use 39 kΩ, a standard value).*

Testing the Amplifier

1. Connect the power supply only after double-checking all connections, especially the transistor leads.

2. Use a VOM to measure the dc voltage from collector to emitter (it should be about 5 V), from base to emitter (0.6-0.7 V), and from collector and emitter to ground (7 V and 2 V, respectively).

3. Replace R1 with the 100 kΩ potentiometer, set to about 39 kΩ. Confirm that all the dc voltages remain about the same. Connect the VOM between collector and ground and observe what happens as R1 is decreased and increased (raising and lowering base current). Use Ohm's Law to determine what is happening to the collector current as you adjust R1. Reset the pot to 39 kΩ.

4. Set the signal (function) generator to output a 1 kHz sine wave of 200 mV_{p-p}, then connect it to C_{in}. If you are using an oscilloscope, you should see a sine wave at the output of C_{out} with an amplitude of about 1 V_{p-p} and inverted (180° of phase shift) with respect to the input. (A VOM measuring ac RMS voltage will show values of about 70 mV RMS at the input and 350 mV RMS at the output—a gain of 5.)

5. Adjust R1 in each direction and observe the output signal with the oscilloscope. As you lower the collector current, you will begin to see the output waveform clip on positive peaks as the collector current is cut off. Raising collector current will eventually result in distortion on negative peaks as the transistor enters the saturation region.

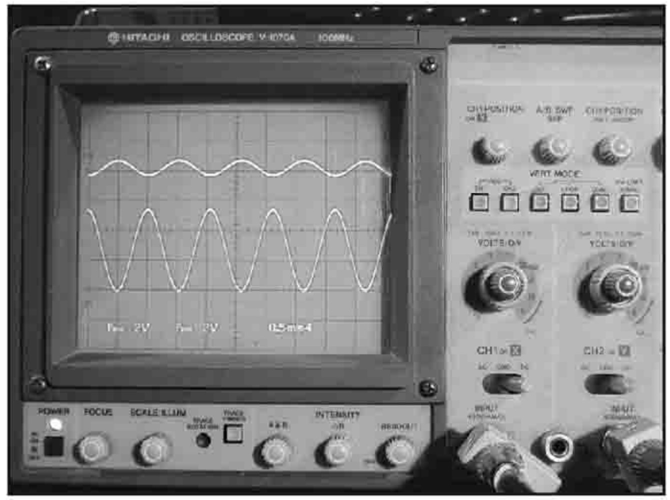

Figure 3—The oscilloscope shows the input (top trace) and output (bottom trace) waveforms. The output is inverted with respect to the input and the voltage gain is approximately 5.

6. Return R1 to 39 kΩ and increase the input signal to observe distortion on the output. If you are using a VOM, note that the RMS output increases more slowly as the signal is clipped.

7. Turn down the input signal as far as possible. Connect the third 10 µF capacitor across R_e. (Connect the negative side of a polarized capacitor to ground.) Slowly increase the input signal and observe the new gain of the circuit. By bypassing R_e, the dc operation of the circuit is unaffected, but now the emitter circuit is effectively grounded for ac signals. The gain is now limited only by the internal impedance of the transistor emitter.

8. Now that you have a working circuit—experiment with it!

- Rework the math for a Q-point with 10 times more and 10 times less collector current.
- Raise and lower the input frequency to see where the gain drops to 70% of the peak value. These are the –3 dB frequencies that determine the amplifier's bandwidth. (These frequencies may be out of range, depending on your instruments.)
- Depending on your generator's capabilities, try different waveforms, such as square or triangle waves, at different frequencies. Does the amplifier faithfully reproduce them?
- Substitute other transistors of the same type and of different types to see what happens to the dc and ac performance.

Suggested Reading

"Transistor Amplifier Design—A Practical Approach" in Chapter 8 of *The ARRL Handbook*. For a more complete discussion of the common emitter amplifier, check out Chapter 2 of *The Art of Electronics*.

Shopping List

You'll need the following components:

- 100 kΩ potentiometer.
- ¼ W resistors of the following values: 270 Ω, 1.5 kΩ, 6.8 kΩ, 39 kΩ.
- 3—10 µF capacitors with a voltage rating of 25 V dc or more (electrolytic or tantalum are fine).
- 2N3904 transistor.

Next Month

The common collector amplifier, also known as the emitter follower, will be the subject of next month's experiment. With the exception of a few more resistor values, you'll be able to reuse the components from this month's exercise. See you then! QST

NØAX

HANDS-ON RADIO

Experiment 106
Effects of Gain-Bandwidth Product

Last month, we discussed gain-bandwidth product (GBW or GBP) and how it affects the ability of an op-amp to amplify signals of different frequencies. That's important, because op-amps are used as the active element in signal processing and filter circuits. What effect does GBW have in that kind of application? We'll use *LTspice* to illustrate the effects of GBW in a band-pass filter circuit as an example of the issues the circuit designer has to consider.

Gain and Q

In the experiment portion of the previous experiment, you built a simple amplifier circuit and substituted op-amps with different GBW to see the effect. Clearly, as GBW increased, so did the gain of the circuit at higher frequencies. What about circuit performance at much lower frequencies? Does GBW affect performance there, as well? Yes!

The effects are most easily seen in band-pass filters because requirements for steep filter "skirts" and narrow bandwidths require a lot of gain. Why do they require a lot of gain? Let's take a look at the multiple-feedback band-pass filter in Figure 1.[1] (This design was created by Jim Tonne, W4ENE, using the professional-level version of his *ELSIE* filter design software.[2]) It shows a two-pole band-pass filter with a center frequency, f_0, of 10 kHz and a bandwidth, BW, of 1 kHz. Thus, the filter's Q is

$$Q = f_0 / BW = 10 \text{ kHz} / 1 \text{ kHz} = 10$$

In this example, the software requires values for f_0 and BW, the capacitor values (using the equal C-method), and the order and type of filter response (second order Chebyshev in this case). Figure 1A is the filter design if an *ideal* op-amp is used. That means an op-amp with an infinite GBW and infinite dc gain. Each filter section has the same gain (A_V = 5.6 dB) and Q (18.24). The section's center frequencies are slightly different: $f_{0\text{-}1}$ = 9.56 kHz and $f_{0\text{-}2}$ = 10.46 kHz. Each section then acts as a narrow filter (Q = 18.24) tuned to a single f_0.

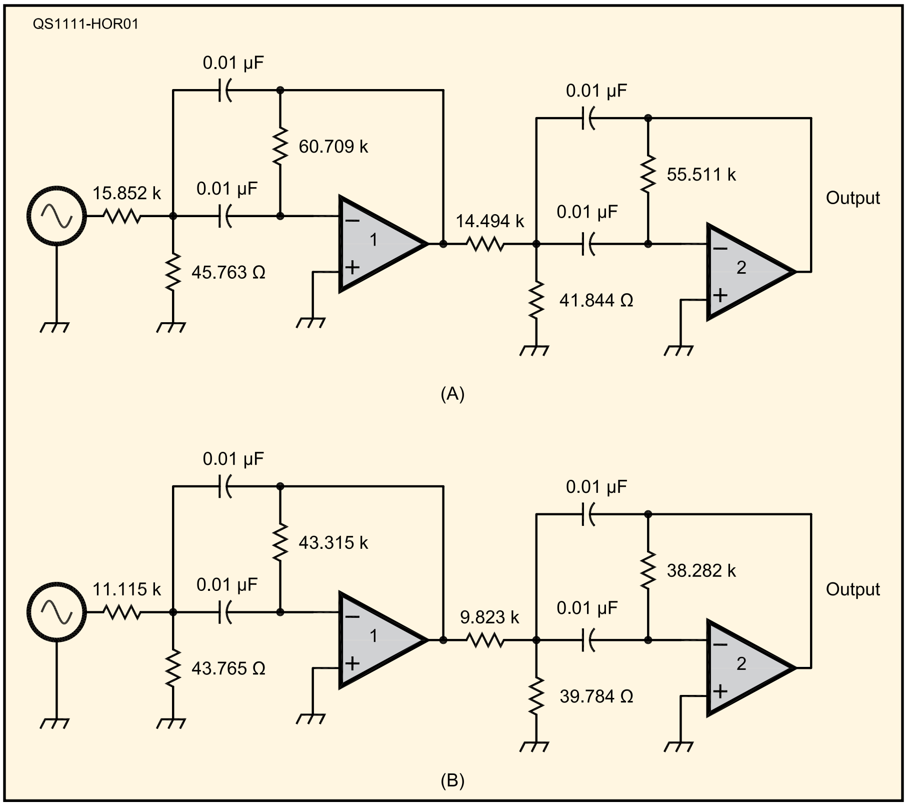

Figure 1 — Schematic of a two pole multiple feedback band-pass filter with a center frequency of 10 kHz and bandwidth of 1 kHz for a Q of 10. (A) shows the design for an ideal op-amp while (B) provides adjustments needed for practical op-amp performance (see text).

If the two filter sections are *cascaded* as shown, the result is the band-pass frequency response as shown in Figure 2. The *pole* for each section is shown by the small, red lines on the frequency axis to either side of 10 kHz. The extra gain is required because the individual filter sections work against each other away from their respective center frequencies. To create the passband of the filter the total response has to add up to 0 dB at the filter's overall center frequency of 10 kHz, which is between the two individual f_0 values. The result is that each filter has to have a gain of greater than 0 dB at its individual f_0.

All well and good, but it's kind of hard to buy an ideal op-amp. They are always out of them when I go to the store! Jim's software, though, allows you to specify the performance of the op-amp and compensates

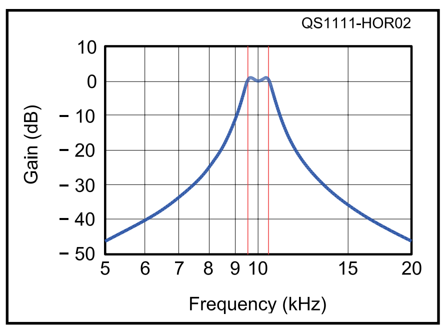

Figure 2 — Frequency response of the filter in Figure 1.

[1]Multiple-feedback band-pass filters are discussed in Hands-On Radio experiment #4. All previous experiments are available to ARRL members at **www.arrl.org/hands-on-radio**.
[2]Tonne Software, **www.tonnesoftware.com**.

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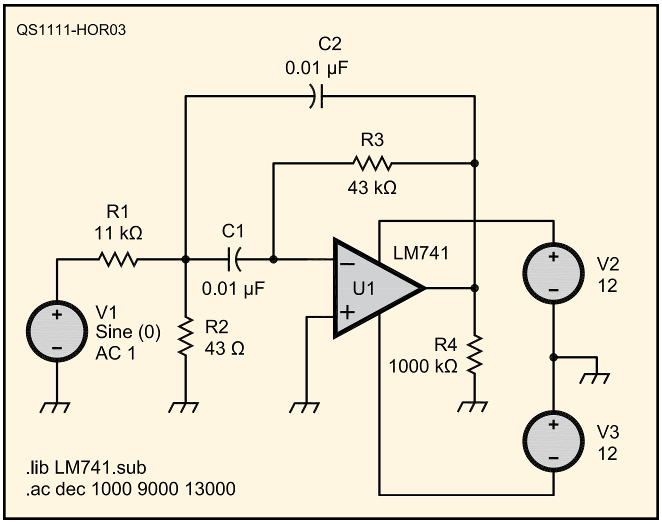

Figure 3 — *LTspice* schematic for Section 1 of the multiple-feedback band-pass filter.

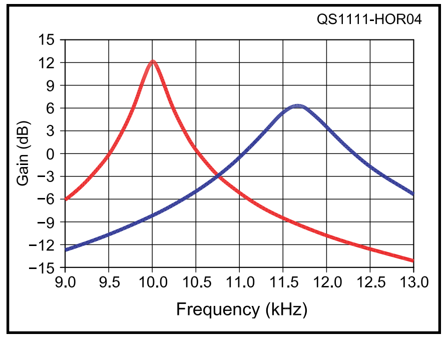

Figure 4 — Frequency response of the filter with an LM741 op-amp (red) and an LM318 op-amp (blue). The higher GBW of the LM318 results in performance that is closer to that of an ideal op-amp.

for its behavior. In this case, Jim used an op-amp with a dc gain of 100 dB (100,000 V/V), a GBW = 1 MHz and an input impedance of 1 MΩ. Figure 1B shows the result — the resistor values are a little smaller and the overall frequency response is the same.

Necessary Gain and Peaking

The non-ideal op-amp selected would seem to have plenty of gain at 10 kHz: 1 MHz / 10 kHz = 100. Each filter section has a gain of about 5.6 dB = 1.9 so we should be in good shape, right? Well, not really. From page 5.70 of the Analog Devices *Op-amp Applications* online book referenced last month: "A rule of thumb is that the open-loop gain of the op-amp should be at least 20 dB (×10) above the amplitude response at the resonant (or cutoff) frequency, including the peaking caused by the Q of the filter… A_0 = H Q, where H is the gain of the circuit."[3] (For a discussion of filter response peaking, see experiment #41.)

If each stage has a gain of 5.6 dB = 1.9 at f_0 and a Q of 18.24, then the op-amp must have a gain of 10 × (1.9 × 18.24) ≈ 348 at f_0. We're short of gain by a factor of about 3.5 to be able to ignore the effects of the op-amp's 1 MHz GBW. That's why the circuit values have to change a little bit.

Why does GBW make a difference at such a low frequency? What happens if the op-amp's GBW is too low? Quoting from page 5.106 of the *Op-amp Applications* book: "Without sufficient…gain, the op-amp virtual ground is no longer at ground. In other words, the op-amp is no longer behaving as an op-amp. Because of this, the [filter] no longer behaves like [a filter]." A virtual ground exists at the op-amp's inverting (–) input *only* if the op-amp's output signal causes all of the currents flowing into and out of those connections to balance. That allows the voltage at the inverting input to be the same as at the non-inverting (+) input, which is connected to ground. If the op-amp doesn't have enough "oomph" (gain and output drive capability) to keep those currents in balance, the inverting input is no longer at ground potential and that invalidates the assumptions on which the filter design equations are based. The circuit may provide some filtering function but it won't perform as designed.

[3]**www.analog.com/library/analogDialogue/archives/39-05/op_amp_applications_handbook.html**

Observing the Effects of GBW

You can simulate Section 1 of the circuit of Figure 1A to see the effects of GBW. Use the closest standard 5% series resistor values, such as 11 kΩ, 43 kΩ, 43 Ω, 10 kΩ, 39 kΩ and 39 Ω. This will shift the center frequency to nearly 12 kHz from the software's precision design. Retrieve the amplifier circuit you simulated for last month's experiment and add the necessary resistor and capacitors to make the multiple-feedback circuit as shown in Figure 3.

To change the values of the components, move the cursor over the symbol until it takes the shape of a hand, right click, then edit the value. (Use "u" for micro.) Start with the LM741 op-amp. You can change the op-amp library model by moving the cursor over the ".lib" library model identification line so that it becomes a text cursor, then right clicking and editing. Don't forget to change the op-amp part number as well, using the same process.

Because we want to see the frequency response of the circuit close to 10 kHz and not spread out from 1 kHz to 1 MHz, edit the simulation command line by right-clicking over the ".ac" line. I found that a span of 9 kHz to 13 kHz made it easy to see the effects of changing the op-amp. Figure 4 shows the result in red. (Click on the horizontal axis cursor to change the plot to linear and use 500 Hz tick marks. Click on the vertical axis cursor to turn off phase plotting.) Now change to the LM318 op-amp used for comparison last month and rerun the simulation. You'll get a response shown in blue in Figure 4 — quite a change!

First, the center frequency shifts from 10.1 kHz and a bandwidth of 300 Hz for the LM741 to 11.7 kHz and 800 Hz with the LM318. Gain also changes from 12 dB with the LM741 to 6 dB with the LM318. Because we're using standard values for the resistors, the design center frequency is now approximately 12 kHz, but the Q and gain values for the LM318 circuit are much closer to what is expected for an ideal op-amp.

You can see the effect even more clearly if you use one of the low cost high GBW op-amps available today, such as the LM7171 with a GBW of 200 MHz. (Download and use the model file as explained last month.) Another way to see big changes in performance is to increase the filter's center frequency. To change f_0 to 100 kHz, reduce the two capacitors by a factor of 100 kHz / 10 kHz = 10 for a value of 0.001 µF. The higher-speed op-amp is required to get anything close to expected performance.

The moral of this story is that sensitive circuits such as moderate- to high-Q filters can be very dependent on the performance of the components used to implement them. Although our junk boxes are full of op-amps with 1, 4 or 10 MHz GBW, they will probably give confusing results in circuits for which they are not suited, or if the tools we use to design the circuits make too many assumptions about their capabilities!

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QST Issue: Mar 2003
Title: Experiment #2--The Emitter-Follower Amplifier
Author: H. Ward Silver, N0AX

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Experiment #2—The Emitter-Follower Amplifier

Our second experiment will again focus on a transistor amplifier—the emitter-follower. This handy amplifier doesn't offer much in the way of voltage gain (it has none), but it provides buffering or isolation for sensitive amplifiers and muscle to output circuits for driving loads like headphones or coaxial cables. It has relatively high input impedance with low output impedance and good *power* gain, as we'll see later.

Background

The emitter-follower (EF) amplifier configuration, also called the common collector, is found in applications where an amplifier must have both high input impedance (to avoid loading a sensitive or low-power circuit) and low output impedance (to drive a heavy load).

The EF provides no voltage gain; in fact, its voltage gain is always less than 1. The collector of the transistor is connected directly to the power supply, without a resistor and the output is taken across the emitter resistor. There is no 180° phase shift as seen in the common-emitter configuration of experiment #1—the output signal follows the input signal with 0° phase shift. This is the origin of the name—the emitter voltage "follows" the input signal voltage.

Why does the EF configuration have a high input impedance? Let's start by looking directly into the base of the transistor at base voltage, V_b and base current, I_b. Remember that β is the transistor current gain, or the ratio of collector to the base current.

$\beta = I_c / I_b$ so $I_c = \beta I_b$

$I_e = I_b + I_c$

Therefore, $I_e = I_b + \beta I_b = I_b (\beta + 1)$

$$V_b = V_{be} + I_e R_e = V_{be} + [I_b (\beta + 1)] R_e \quad [1]$$

The base impedance, Z_b, is the ratio of the change (Δ) in V_b to the resulting change in I_b. Biasing will keep the transistor current "turned on" so V_{be} doesn't change much and can be treated as constant. So, small changes in V_b due to the input signal will cause a corresponding change in I_b.

$$\Delta V_b \approx \Delta I_b \; (\beta + 1) \, R_e \text{ and...} \quad [2]$$

$$Z_b = \Delta V_b \, / \, \Delta I_b \approx (\beta + 1) \, R_e \quad [3]$$

This equation shows that the small changes in I_b amplified by β effectively also multiplies R_e by the same amount. The base impedance (not counting the biasing network R1 and R2) is essentially the current gain, β, multiplied by the emitter resistor, R_e.

The input source doesn't just drive the base, of course; it also has to drive the combination of R1 and R2, the biasing resistors. From an ac point of view, both R1 and R2 can be considered as connected to "ac ground" (the power supply supplies a constant dc voltage; it should present a low impedance, which is effectively an ac short) and they can be treated as if they were connected in parallel. When R1 // R2 are considered along with the transistor base impedance, Z_b, the impedance the input signal source "sees" is:

$$Z_{in} = R1 \,//\, R2 \,//\, Z_b = 1 \,/\, [1/R1 + 1/R2 + 1/R_e (\beta + 1)] \quad [4]$$

Let's figure the output impedance, Z_{out}, too. Looking back into the connection between the transistor emitter and R_e, Z_{out} is made up of three components. The first is R_e, which is connected to ground. The second, Z_e, is the series combination of the transistor's internal emitter impedance, r_e, (note the lowercase "r" which distinguishes it from the external resistance, R_e) and the combined impedance of the signal source, R_s, and the biasing resistors R1 and R2. Using the same explanation of current gain's effect on input impedance—in reverse this time—the impedance presented at the emitter, Z_e, is:

$$Z_e = (R_s \,//\, R1 \,//\, R2) \,/\, (\beta + 1) + r_e \quad [5]$$

From the physics of silicon transistors, at room temperature, r_e = 25 mV / I_{eq}, where $I_{eq} \approx I_{cq}$ in mA, so, for most designs, r_e will be much less than 50 Ω. Similarly, in our experiment, R1 and R2 are likely to be much higher than R_s, the signal source impedance—which is usually less than 1 kΩ. When R_e and Z_e are combined, the output impedance of the circuit becomes:

$$Z_{out} = Z_e \,//\, R_e \quad [6]$$

We see, therefore, that our emitter follower has a relatively high input impedance and a low output impedance, making it ideal for driving low-impedance loads.

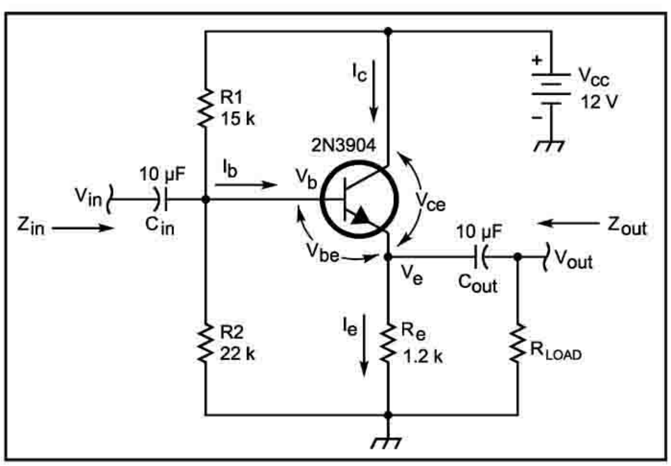

Figure 1—The common emitter circuit. This is a current or power amplifier, offering high input impedance and low output impedance. It is useful for driving low impedance loads, buffering and isolation.

Terms to Learn

Input (Output) Impedance—the equivalent ac impedance looking into the input (output) of a circuit.

Cascade—two circuits connected such that the output of the first is connected to the input of the second.

Power Gain—the ratio of output power to input power.

Buffer—an amplifier used to provide isolation between two circuits.

//—in parallel with.

Key Equations

$$I_c \approx I_e, \; I_c = I_b \beta \quad [7]$$

$$V_{cc} \approx V_{ce} + I_c R_e \quad [8]$$

$$V_b \approx V_{be} + I_c R_e \quad [9]$$

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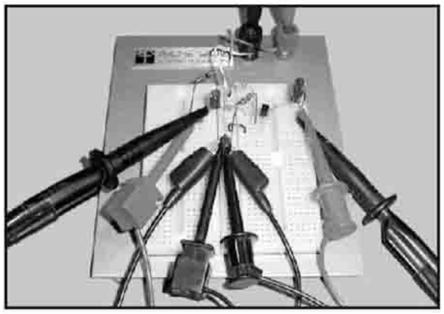

Figure 2—This photo shows the construction of the EF (emitter follower) circuit. Note that the input connection is on the right and the output connection is on the left. This keeps the input and output leads away from each other and helps prevent oscillation. All ground leads (black clips) are connected together at a single point.

Figure 3—An oscillating circuit—with a 1 kHz sine wave input, both the input (top) and output (bottom) signals show significant oscillation at more than 1 MHz. Experiment with lead placement and circuit component placement to learn what causes and prevents oscillation.

Designing the Amplifier

Choose the circuit's operating requirements:

V_{cc} = 12 V *(our power supply voltage)*

Q-point of I_{cq} = 5 mA and V_{ceq} = 6 V *(rule of thumb, ½ V_{cc} allows the maximum output voltage swing)*

Assume the transistor's β is 150 and base-to-emitter voltage, V_{be} = 0.7 V

1. $R_e = (V_{cc} - V_{ceq}) / I_{cq}$ = 1.2 kΩ *(Eq 8)*
2. Base current, $I_b = I_{cq} / \beta$ = 33 µA *(Eq 7)*
3. Current through R1 and R2 = 10 I_b = 330 µA *(a rule of thumb simplifying calculations and keeping I_b stable with a "stiff" bias supply).*
4. Voltage across R2 = $V_{be} + I_c R_e$ = 0.7 + 5 mA (1.2 kΩ) = 6.7 V *(Eq 9)*

R2 = 6.7 V / 330 µA = 20.3 kΩ (use 22 kΩ). *(Ohm's Law)*

5. Voltage across R1 = V_{cc} – 6.7 V = 5.3 V. *(Voltage divider)*

R1 = 5.3 V / 330 µA = 16.06 kΩ (use 15 kΩ). *(Ohm's Law)*

$Z_{in} = 1 / [1/R1 + 1/R2 + 1/R_e (\beta + 1)] \approx$ 8.5 kΩ *(Eq 4)*

Assuming R_s = 50 Ω, $Z_{out} \approx r_e // R_e$ = 5 Ω // 1.2 kΩ ≈ 4.99 Ω *(Eq 5 and 6)*

That's where our emitter follower shines!

Testing the Amplifier

Connect the power supply after double-checking all connections, especially the transistor leads. Figure 2 shows the breadboard circuit.

1. Use a VOM to measure the dc voltage from collector to emitter (it should be about 6 V), from base to emitter (0.6 – 0.7 V) and from emitter to ground (6 V). Replace R1 with a 100 kΩ potentiometer, set to 15 kΩ. Start with a value of 10 kΩ for R_{load}.

2. Set the signal generator to output a 1 kHz sine wave at 1 V_{p-p}, then connect it to C_{in}. You should see a sine wave at the output of C_{out} with an amplitude of about 1 V_{p-p} and in phase with the input. (A VOM measuring ac voltage will show 700 mV rms at the input and output.)

3. You will find later that the emitter follower has a very high bandwidth. This can lead to oscillation at several hundred kHz or higher, if you're not careful. This instability is visible as the "fuzzy" oscilloscope trace shown in Figure 3. Those of you using voltmeters only might see intermittent or jumpy ac signal voltages. It's important to keep input leads away from output leads and use the single-point ground as shown in the breadboard circuit of Figure 2. Sometimes, just moving the leads around will cause the oscillation to start and stop, so don't be afraid to experiment.

4. Increase the input signal to 5 V_{p-p}. Adjust R1 in each direction and observe the output signal with the oscilloscope. As you lower the collector current (V_b decreasing), you will see the output waveform clip on negative peaks as the collector current is cut off. Raising collector current will eventually result in distortion on positive peaks as the transistor enters saturation.

5. Substitute 1 kΩ, 100 Ω, and 10 Ω resistors for R_{load}, reducing the input voltage at each value, so that the output waveform remains undistorted. Lower resistance loads can only be driven at lower voltages because the ac currents in the transistor are much higher at lower values of load resistance. You can read about ac load lines in the reference texts for a detailed explanation. You'll also see the output signal begin to "lag" behind the input signal at these low load values. Why? The impedance of the output coupling capacitor at 1 kHz becomes significant for loads below 100 Ω, introducing phase shift in a series RC circuit.

6. If the input power is $(V_{in})^2 / Z_{in}$ and the output power is $(V_{out})^2 / R_{load}$, compute the power gain of the amplifier for the maximum undistorted values of input and output voltage at the different loads.

$$\text{Power Gain} = P_{out} / P_{in} = [(V_{out})^2/R_{load}]/[(V_{in})^2/Z_{in}] \qquad [10]$$

If $V_{in} \approx V_{out}$, then power gain = Z_{in} / R_{load} ! See how closely this approximation agrees with your measurements.

7. Now that you have a working circuit—experiment with it!

- Rework the math for a Q-point with 5 times more and 10 times less collector current. Calculate Z_{in} and Z_{out} for those currents.
- Raise the input frequency to see if you can find where the gain drops to 70% of the peak value; this is the upper –3 dB frequency of the amplifier.
- Drive both the CE and EF amplifiers with a square-wave at the highest frequency your generator can reach, using a 1 kΩ load resistor. Use the 'scope to determine which circuit will follow the input more accurately thus indicating wider bandwidth.

Suggested Reading

- "Transistor Amplifier Design—A Practical Approach" in Chapter 8 of *The ARRL Handbook*.
- "Low-Frequency Transistor Models" in Chapter 10 of The *ARRL Handbook*.
- For a more complete discussion of the Emitter-Follower amplifier, check out Chapter 2 of *The Art of Electronics*, by Horowitz and Hill.

Shopping List

You'll need the following components:

- 100 kΩ potentiometer.
- ¼ W resistors of the following values: 10 Ω, 100 Ω, 1 kΩ, 1.2 kΩ, 10 kΩ,15 kΩ, 22 kΩ.
- 2-10 µF capacitors with a voltage rating of 25 V dc or more (electrolytic or tantalum are fine).
- 2N3904 transistor.

Next Month

We shift gears next month to operational amplifiers—usually known by their nickname "op amps." Be prepared to buffer, invert, add and subtract! QST

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QST Issue: Jan 2004
Title: Experiment #12--Field Effect Transistors
Author: H. Ward Silver, N0AX

Experiment #12—Field Effect Transistors

Welcome to the second year of "Hands-On Radio." After an introduction and 11 experiments, we've covered a lot of ground but it seems like we've only scratched the surface! Radio electronics is a pretty broad field, so there are lots of experiment topics remaining.

The field effect transistor, or FET, is an attractive replacement for bipolar transistors in switches and amplifiers. Why? The FET offers high input impedance, excellent gain, and easy biasing. We'll revisit the first "Hands-On Radio" experiment and find out how these characteristics fit the common-emitter design.

Terms to Learn

- *Transconductance*—The measure of change in output current caused by a change in input voltage.
- *Channel*—The semiconductor material between an FET drain and source through which current flows.
- *Enhancement and depletion mode*—In enhancement-mode FETs, increasing gate voltage causes channel conductivity to increase. For depletion-mode FETs, the opposite is true.
- *On-resistance*—The drain-to-source resistance of an FET's channel at maximum conductivity.

Background

While you may know that John Bardeen, Walter Brattain and William Shockley constructed the first bipolar transistor in 1948, you may not know that the idea behind the FET was patented in 1926 by Julius Lilienfield. A working (but very slow) amplifier was made using salt by Robert Pohl in 1938. The FET is actually the oldest transistor and its operation is much closer to the vacuum tube than the bipolar transistor.

Figure 1 shows the rudimentary construction and symbols for the two primary types of FETs, the junction FET (JFET) and the metal-oxide-semiconductor FET (MOSFET), that we met in experiment #9. Metal electrodes attach leads to the semiconductor material. The junction in a JFET is formed by the different material types (P and N) of the gate and the channel. MOS describes the construction of the gate; a metal electrode coating an insulating layer of oxide (usually quartz, silicon dioxide or SiO_2) which, in turn, contacts the channel material directly. FET and bipolar transistors have terminals with similar functions—gate and base, collector and drain, and emitter and source.

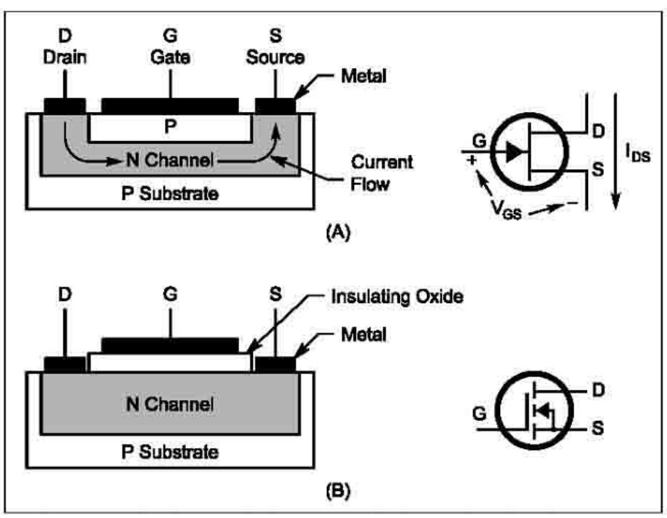

Figure 1—JFET (A) and MOSFET (B) construction are shown along with their symbols. N-channel, enhancement-mode devices are shown.

Where the bipolar transistor uses input current to control output current, the FET uses input voltage. In place of the bipolar transistor's pair of P-N junctions placed back-to-back between collector and emitter, the FET has a *channel* of either P-type or N-type material. In the bipolar transistor, current flows from the base to emitter, controlling current flow through the two P-N junctions. In the FET, gate voltage changes the conductivity of the channel and so the current flowing between drain and source also changes. Very little current flows in the gate of an FET.

Like the bipolar transistor's NPN and PNP devices, the FET comes in different flavors, but it has *four* instead of two. Figure 1 shows N-channel devices, but the channels can be made of either N or P-type material and the device can be designed so that increasing gate voltage causes more or less current to flow in the channel. If more channel current flows with increasing gate voltage, it is an *enhancement-mode* device. Conversely, *depletion-mode* devices have less current with increasing gate voltage. The most widely used device is the N-channel enhancement-mode FET.

The change in output current caused by a change in input voltage is called *transconductance*. Analogous to a bipolar transistor's current gain or beta, its symbol is g_m and its units are siemens (S) because it measures the ratio of current to voltage.[1] The input voltage, V_{GS}, is measured between the FET gate and source. The output current, I_{DS}, flows from drain to source.

$$g_m = \Delta I_{DS} / \Delta V_{GS} \text{ and } \Delta I_{DS} = g_m \Delta V_{GS} \quad \text{[Eq 1]}$$

The voltage gain of the FET amplifier in Figure 2 depends on the FET transconductance because varying the current in the FET drain causes a varying voltage across the drain resistance. The model for the FET is the variable resistive divider shown in Figure 2A, with V_{GS} controlling the value of R_{DS}. If V_O is measured at the drain terminal (just as the common-emitter output voltage is measured at the collector), then

$$\Delta V_O = -\Delta I_{DS}\, R1 = -g_m \Delta V_{GS}\, R1 \quad \text{[Eq 2]}$$

Substituting this relationship gives voltage gain in terms of transconductance and the drain load:

$$A_V = \Delta V_O / \Delta V_{GS} = -g_m\, R1 \quad \text{[Eq 3]}$$

[1]Siemens (pronounced "see-mins") is the international unit for conductance, formerly mhos. Its symbol is a capital "S" and 1 siemens = 1 A/V.

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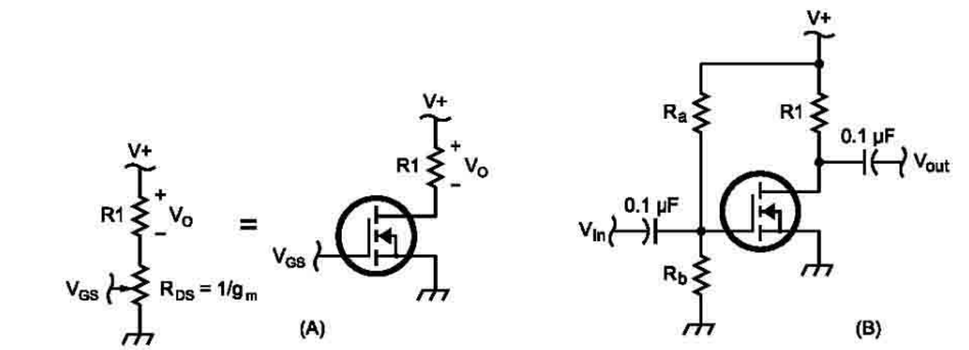

Figure 2—(A) A MOSFET common-source amplifier can be modeled as a variable voltage divider between the drain load and the FET. (B) A simple MOSFET amplifier with a voltage divider for supplying gate bias.

The minus sign results from the output voltage decreasing as drain current increases, just as with the common-emitter amplifier.

A key difference between the FET and bipolar transistor is that the channel of an FET acts like a variable resistance. That means that drain-to-source voltage can become quite low—lower than a completely saturated bipolar transistor's V_{CE}. Note that the *on-resistance* for power FETs can be very low—in the milliohm range. This allows them to switch heavy loads while dissipating little power. In amplifiers, this also allows more output voltage swing.

Another important parameter of FETs is the gate-to-source voltage at which no more current flows through the channel. This is called the *pinch-off voltage*, V_P. Imagine the gate voltage as a pair of fingers tightening or loosening around a hose carrying a stream of water and you'll have a pretty good idea of the mechanics involved. When V_{GS} reaches V_P, the area of the channel through which current flows is reduced to zero. Depending on the type of FET, V_P can be positive or negative. Switching MOSFETs are generally designed to have V_P greater than zero to make interfacing with digital logic easier. The voltage at which the MOSFET begins to conduct current is usually shown as $V_{GS(TH)}$, the *gate threshold voltage.*

Testing a MOSFET Common-Source Amplifier

This experiment will use a common switching MOSFET, the IRF510. This is a large transistor capable of handling several amps of drain current, but it demonstrates the mechanics of MOSFET amplifiers well. You may want to download the data sheet for the transistor.[2]

- When using a single power supply, it's necessary to bias the gate so that output voltage can both increase and decrease. Bias is supplied by R_a and R_b which act as a voltage divider—$V_{GS} = R_b / (R_a + R_b)$. For the divider, use a 10 kΩ potentiometer with the wiper connected to the FET gate and the remaining leads connected to V+ and ground. Start with the potentiometer set so that the wiper is nearly at ground voltage. Leave the input signal source disconnected.
- The IRF510 can handle a lot of current, but we'll limit drain current to 12 mA by using a 1 kΩ resistor for R1.
- Monitor the FET drain voltage and slowly adjust the bias pot so that gate voltage increases. When the gate threshold voltage is reached, the FET will start conducting and drain voltage will fall rapidly to zero. Record the gate threshold voltage as well as the voltage when the FET drain is 1 V below V+ and 1 V above ground.
- Set the signal generator to output a 0.1 $V_{p\text{-}p}$ 1 kHz sine wave. Set the bias voltage halfway between $V_{GS(TH)}$ and V+. Connect the input signal. Observe the output voltage and experiment by adjusting the bias voltage to get the largest undistorted output.
- Calculate voltage gain, $A_v = -$ (drain voltage change) / (gate voltage change) and transconductance, $g_m = - A_v / R1$. My FET showed a voltage gain of –18 and a transconductance of 0.018 S.
- Experiment by varying R1 and observing the effect on voltage gain. Readjust the bias setting and input voltage to get the maximum undistorted output voltage for each value of R1.

You may be asking yourself why your measured transconductance is so low compared to the specified minimum of 1.3 S in the data sheet. The answer lies in the graph of transconductance versus drain current (Figure 12 in the data sheet). The IRF510 transconductance is optimized for drain currents of several amperes and it falls off drastically at low currents.

Suggested Reading

Begin by reading the ARRL *Handbook* sections on FETs, beginning on pages 8.23 and 10.32. *The Art of Electronics* devotes all of Chapter 3 to FETs, with sections 3.07 and 3.08 covering amplifier design.

Shopping List

- IRF510 transistor (RadioShack 276-2072)
- 10 kΩ potentiometer (multi-turn preferred, but not required)
- Two 0.1 µF capacitors
- 1 kΩ, ¼ W resistor

Next Month

We have focused on active circuits throughout the first year of "Hands-On Radio." It's time to consider a passive circuit for a change. Next month, we'll explore several types of attenuators and their design equations.

The Hands-On Radio Web site is **www.arrl.org/tis/info/html/hands-on-radio/**.

[2]The IRF510 data sheet may be downloaded from **www.rigelcorp.com/__doc/8051/IRF510.pdf**. (Note: There are two consecutive underscores prior to "doc.")

FEEDBACK

◊ Experiment #12 of "Hands-On Radio" [Jan 2004, Figure 2, page 62], should show V_o with its "+" sign at the bottom of R1 and referenced to ground. This will then be consistent with Equation 2.—*tnx Jason Dugas, KB5URQ* that is much larger than I_b (to eliminate effects of β variation). V_b should be much larger than ΔV to reduce the effects of variations in ΔV.

Three additional biasing schemes are presented in **Fig 6.50**. All provide bias that is stable regardless of device parameter variations. A and B require a negative power supply. The circuit of Fig 6.50C uses a second, PNP, transistor for bias control. The PNP transistor may be replaced with an op amp if desired. All three circuits have the transistor emitter grounded directly. This is often of great importance in microwave amplifiers. These circuits may be analyzed using the simple model of Fig 6.49.

The biasing equations presented may be solved for the resistors in terms of desired operating conditions and device parameters. It is generally sufficient, however, to repetitively analyze the circuit, using standard resistor values.

The small-signal transconductance of a common-emitter amplifier was found in the previous section. If biased for constant current, the small-signal voltage gain will vary inversely with temperature. Gain may be stabilized against temperature variations with a biasing scheme that causes the bias current to vary in *proportion to absolute temperature*. Such methods, termed PTAT methods, are often used in modern integrated circuits and are finding increased application in circuits built from discrete components.

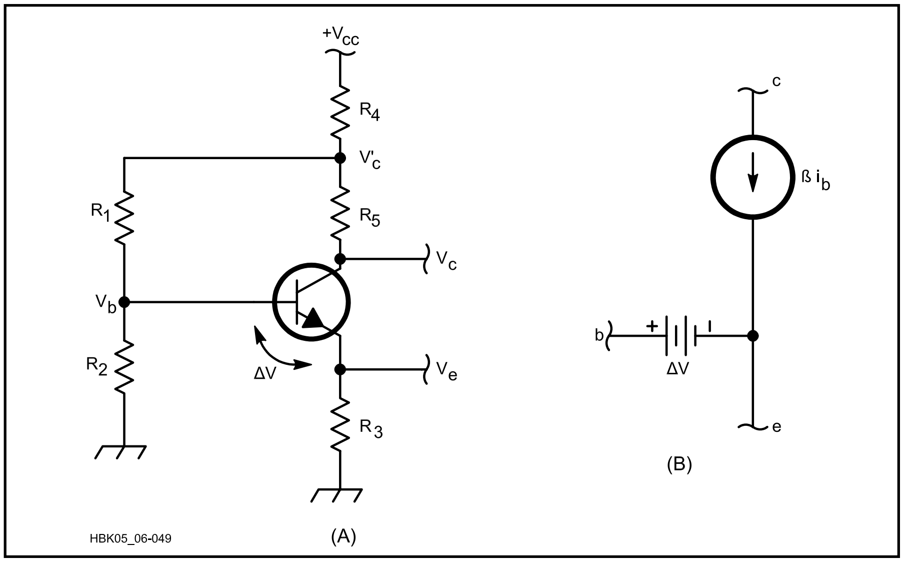

Fig 6.49—(A) Circuit used for evaluation of transistor biasing. (B) The model used for bias calculations.

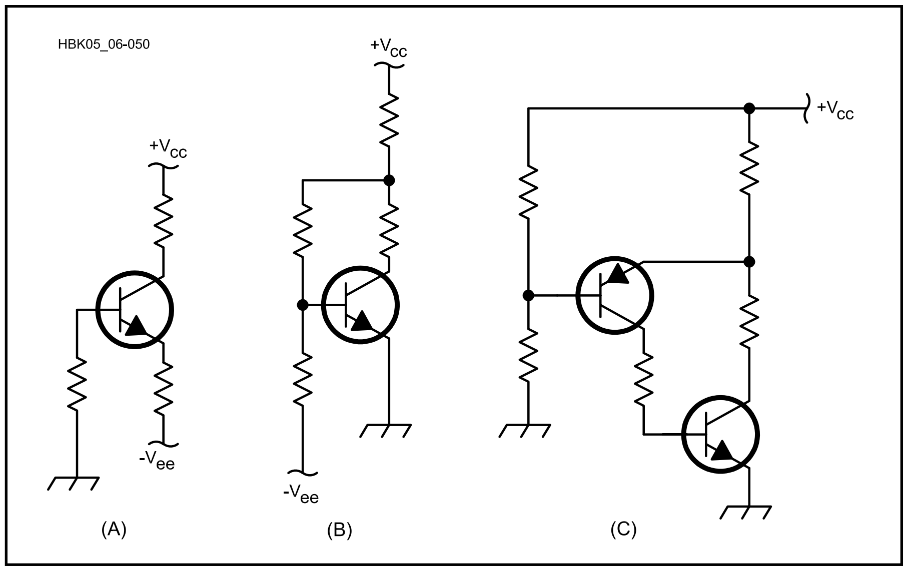

Fig 6.50—Alternative biasing methods. (A) and (B) use dual power supplies, (B) and (C) allow the emitter to be at ground while still providing temperature-stable operation.

Large-Signal Operation

The models presented in previous sections have dealt with small signals applied to a bipolar transistor. While small-signal design is exceedingly powerful, it is not sufficient for many designs. Large signals must also be processed with transistors. Two significant questions must be considered with regard to transistor modeling. First, what is a reasonable limit to accurate application of small-signal methods? Second, what are the consequences of exceeding these limits?

The same analysis of the Ebers-Moll model yields an equation for collector current. The mathematics show that current will vary in a complicated way, for the sinusoidal signal voltage is embedded within an exponential function. Nonetheless, the output is a sinusoidal current if the signal voltage is sufficiently low.

The current of the equation may be studied by normalizing the current to its peak value. The result is relative current, I_r, which is plotted in **Fig 6.51** for V_p values of 1, 10, 30, 100, and 300 mV. The 1-mV case is very sinusoidal. Similarly, the 10-mV curve is generally sinusoidal with only minor distortions. The higher amplitude cases show increasing distortion.

Constant base-voltage biasing is unusual. More often, a transistor is biased to produce nearly constant emitter current. When such an amplifier is driven by a large input signal, the average bias voltage will adjust itself until the time average of the nonlinear current equals the previous constant bias current. Hence, it is vital to consider the average relative current of the waveforms of Fig 6.51. This is evaluated through calculus.

The average relative currents for the cases analyzed occur at the intersection of the curves with the dotted lines of Fig 6.51.

Ready-Made Models

Many manufacturers provide computer models, S-parameter files or other data helpful when including their devices in circuits modeled with *SPICE* and other computer tools. These files are often available from component manufacturers' Web sites, from software providers, or from third parties. Because this information changes, use your favorite Internet search tool to look for information on components of interest.

For example, the dotted curve intersects the V_p = 300-mV waveform at an average relative current of 0.12. If an amplifier was biased to a constant current of 1 mA, but was driven with a 300-mV signal, the positive peak current would reach a value greater than the average by a factor of 1/(0.12). The average current would remain at 1 mA, but the positive peak would be 8 mA. The transistor would not conduct for most of the cycle.

The curves have presented data based upon the simplest of large-signal models, the Ebers-Moll equation. Still, the simple model has yielded considerable information. The analysis suggests that a reasonable upper limit for accurate small-signal analysis is a peak base signal of about 10 mV. The effect of emitter degeneration is also evident. Assume a transistor is biased for $r_e = 5\ \Omega$ and an external emitter resistor of 10 Ω is used. Only the r_e portion of the 15 Ω total is nonlinear. Hence, this amplifier would tolerate a 30-mV signal while still being well described with a small-signal analysis.

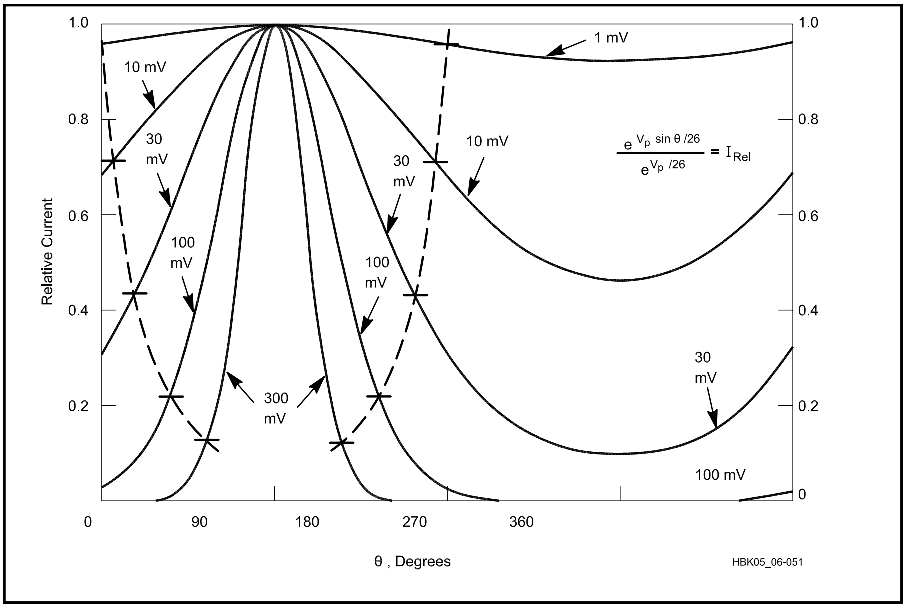

Fig 6.51—Normalized relative current of bipolar transistor under sinusoidal drive at the base.

FETS

An often used device in RF applications is the field-effect transistor (FET). There are many kinds: JFETs, MOSFETs and so on. Here we will discuss JFETs, with the understanding that other FETs are similar.

We viewed the bipolar transistor as controlled by either voltage or current. The JFET, however, is purely a voltage controlled element, at least at low frequencies. The input gate is usually a reverse biased diode junction with virtually no current flow. The drain current is related to the source-gate voltage by:

$$I_D = I_{DSS}\left(1 - \frac{V_{sg}}{V_p}\right)^2 \qquad 0 \le V_{sg} \le V_p$$

$$I_D = 0 \qquad V_{sg} > V_p \qquad (26)$$

where I_{DSS} is the drain saturation current and V_p is the pinch-off voltage. Operation is not defined when V_{sg} is less than zero because the gate diode is then forward biased. Equation 26 is a reasonable approximation as long as the drain bias voltage exceeds the magnitude of the pinch-off voltage.

Biasing FETs

Two virtually identical amplifiers using N-channel JFETs are shown in **Fig 6.52**. The two circuits illustrate the two popular methods for biasing the JFET. Fixed gate-voltage bias, Fig 6.52A, is feasible for JFETs because of their favorable temperature characteristics. As the temperature of the usual FET increases, current decreases, avoiding the thermal-runaway problem of bipolar transistors.

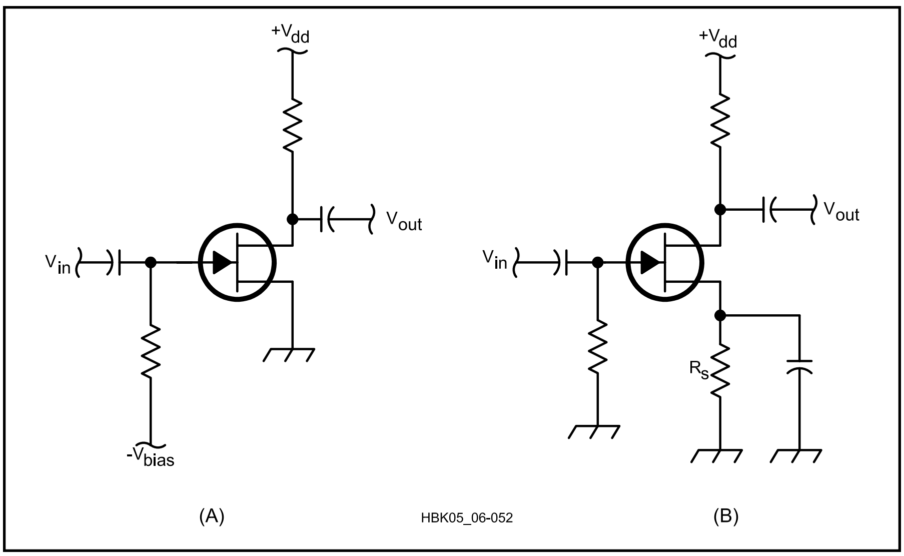

Fig 6.52—Biasing schemes for a common-source JFET amplifier. $-V_{bias}$ is normally adjusted to suit each device; there is a significant spread over a product run. Also note that some FETs can exhibit thermal runaway in some current/temperature ranges.

A known source resistor, R_s in Fig 6.52B, will lead to a known source voltage. This is obtained from a solution of equation 26 (see **Eq 27**).

The drain current is then obtained by direct substitution.

$$V_{sg} = \frac{\left[\frac{1}{R_s I_{DSS}} + \frac{2}{V_p}\right] - \left[\left(\frac{1}{R_s I_{DSS}} + \frac{2}{V_p}\right)^2 - \left(\frac{2}{V_p}\right)^2\right]^{0.5}}{\frac{2}{V_p^{\,2}}} \qquad (27)$$

Alternatively, a desired drain current less than I_{DSS} may be achieved with a proper choice of source resistor

$$R_s = \frac{V_p\left(1-\frac{I_D}{I_{DSS}}\right)^{0.5}}{I_D} \qquad (28)$$

The small-signal transconductance of the JFET is obtained by differentiating equation 26

$$g_m = \frac{dI_D}{dV_{sg}} = \frac{-2\,I_{DSS}}{V_p}\left(1-\frac{V_{sg}}{V_p}\right) \qquad (29)$$

The minus sign indicates that the equation describes a common-gate configuration. The amplifiers of Fig 6.52 are both common-source types and are described by equation 29 except that g_m is now positive. Small-signal models for the JFET are shown in **Fig 6.53**. The simple model is that inferred from the equations while the model of Fig 6.53B contains capacitive elements that are effective in describing high-frequency behavior. Like the bipolar transistor, the JFET model will grow in complexity as more sophisticated applications are encountered.

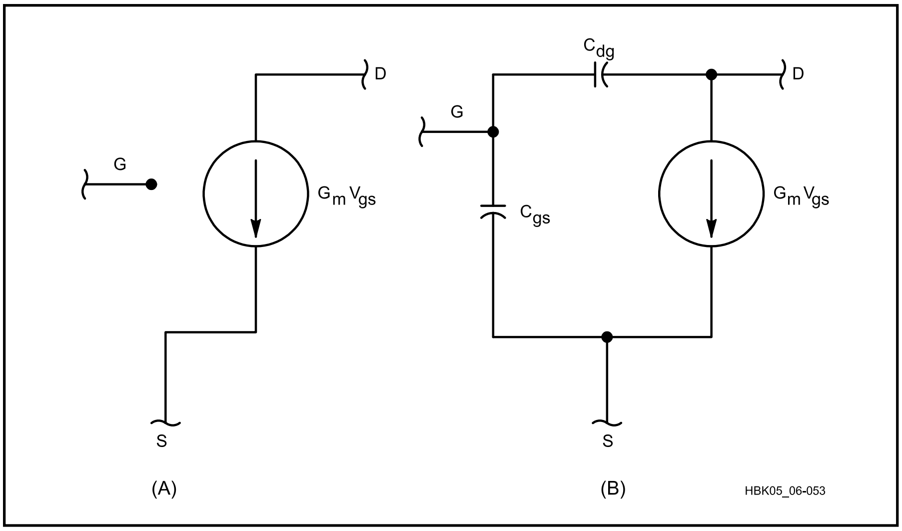

Fig 6.53—Small-signal models for the JFET. (A) is useful at low frequency, (B) is a modification to approximate high-frequency behavior.

Large-Signal Operation

Large-signal JFET operation is examined by normalizing the previous equation to $V_p = 1$ and $I_{DSS} = 1$ and injecting a sinusoidal signal. The circuit is shown in **Fig 6.54**. Also shown in the figure are examples for a variety of bias and sinusoid amplitude conditions. The main feature is the asymmetry of the curves. The positive portions of the oscillations are farther from the mean than are the negative excursions. This is especially dramatic when the bias, v_0, is large, which places the quiescent point close to pinch-off. With such bias and high-amplitude drive, conduction occurs only over a small fraction of the total input waveform period.

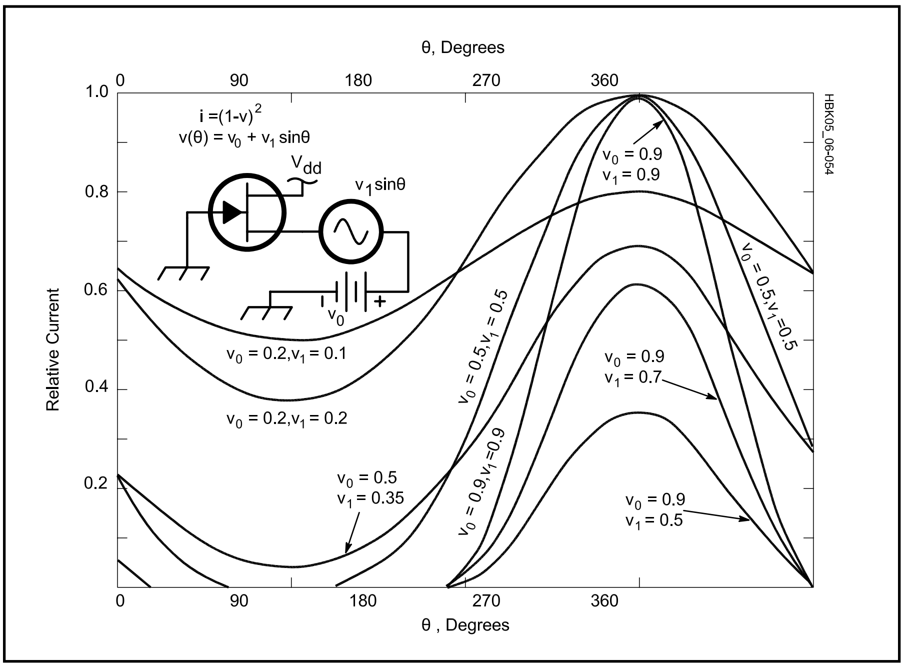

Fig 6.54—Relative normalized drain current for a JFET with constant voltage bias and sinusoidal signals. Relatively "clean" waveforms exist for low signals while large input amplitudes cause severe distortion.

The average current for these operating conditions can be determined by calculus. The average current values obtained may be further normalized by dividing by the corresponding dc bias current, $I_0 = (1 - v_0)^2$. The results are shown in **Fig 6.55**. The curves show that the average current increases as the amplitude of the drive increases. This, again, is most pronounced when the FET is biased close to pinch-off.

Although practical for the JFET, constant-voltage operation in the previous curves is not common. Instead, a resistive bias is usually employed, Fig 6.52B. With this form of bias, the increased current from high signal drive will cause the voltage drop across the bias resistor to increase. This will then move the quiescent operating level

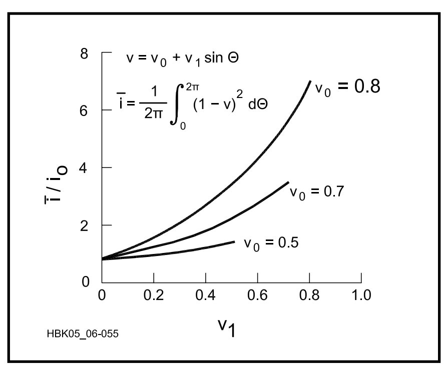

Fig 6.55—Change in average current of a JFET with increasing input signals. The average current with no input signals is I_0, while v_1 is the normalized drive amplitude, and v_0 is the bias voltage.

closer to pinch-off, accompanied by a reduced small-signal trans-conductance. This behavior is vital in describing the limiting found in FET oscillators.

The limits on small-signal operation are not as well defined for a FET as they were for the bipolar transistor. Generally, a maximum voltage of 50 to 100 mV is allowed at the input (normalized to a 1-V pinch-off) without severe distortion. The voltages are much higher than they were for the bipolar transistor. However, the input resistance of the usual common source amplifier is so high and the corresponding transconductance low enough that the available gain is no greater than could be obtained with a bipolar transistor. The distortion is generally less with FETs, owing to the lack of high-order curvature in the defining equations.

Many of the standard circuits used with bipolar transistors are also practical with FETs. Noting that the transconductance of a bipolar transistor is $g_m = I_e$ (dc mA) / 26, the previous equations may be applied directly. The "emitter current" is chosen to correspond with the FET transconductance. A very large value is used for current gain. The same calculator or computer program is then used directly. In practice, much higher terminating impedances are needed to obtain transducer gain values similar to those of bipolar transistors.

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Suggested Additional Reading

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Notes

[1]Superconducting circuits are the one exception; but they are outside the scope of this book.

[2]There are numerous manufacturers of excellent heat sinks. References to any one manufacturer are not intended to exclude the products of any others, nor to indicate any particular predisposition to one manufacturer. The catalogs and products referred to here are from: Wakefield Thermal Solutions, Inc., 33 Bridge Street, Pelham, NH 03076, Phone: (603) 635-2800.

NØAX

HANDS-ON RADIO

Experiment #77 — Load Lines

Once past the very basic levels of transistor amplifier circuits, you'll encounter the *load line*, a graphical method of circuit design. This experiment shows you how the load line is determined and applied to circuit behavior.

Diode Load Line

A diode is the simplest semiconductor device for which a load line can be drawn. Figure 1(A) shows a diode in series with a resistor load, R_L. For any given combination of V_S and R_L, if we know the diode's forward voltage, V_F, we can solve for the diode current, $I_F = (V_S - V_F) / R_L$. V_F, however, depends on I_F, so we must solve the exponential equation for I_F as a function of V_F, shown as the diode's *characteristic I-V* curve in Figure 1(B).[1]

Figure 1(B) also shows the less precise, but easier to use, graphical method of load lines. The load line describes what happens to voltage and current in R_L. It is drawn between the maximum and minimum possible values of current and voltage across R_L. For example, if $I_F = 0$, there is no voltage drop across the diode and the voltage across R_L is V_S — that's point A on the load line. Similarly, if $V_F = 0$, then $I_F = V_S/R_L$ and that's point B on the load line.

[1]The Fundamental Diode Equation is presented in the "Analog Basics" chapter of any recent *ARRL Handbook*.

The only point at which the load line intersects the curve is point C — the *operating point* for the circuit. The intersection is the solution of the diode's characteristic curve equation with the known value of R_L and V_S. If either V_S or R_L change, the slope or placement of the load line will change along with its intersection with the diode's characteristic curve. Let's try it!

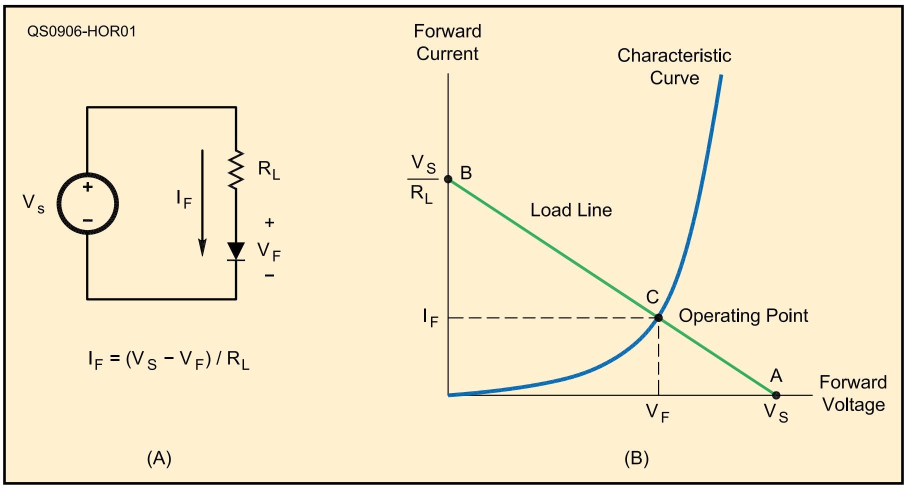

Figure 1 — The simple circuit at (A) can be used to determine the diode's characteristic curve at (B). The intersection of the load line and the characteristic curve is the circuit's operating point.

Operating Point Control

Build the circuit in Figure 1(A) using a 1N4001 silicon diode rectifier, $V_S = 3$ V, and $R_L = 1$ kΩ. Prepare a graph with the I_F axis showing 0 to 50 mA and the V_F axis showing 0 to 10 V. Draw the load line between point A ($I_F = 0$ mA, $V_F = V_S = 3$ V) and point B ($I_F = V_S / R_L = 3$ mA, $V_F = 0$ V).

Measure the diode's forward voltage, V_F, and use Ohm's Law to calculate I_F from the voltage across R_L or measure it directly with a meter. The values should be somewhere around 0.6 V and 2.4 mA. When that point is plotted, it should be very close to or on the load line.

Vary V_S from 1 to 10 V in steps of 1 V, calculating point A and B and drawing a new load line at each step. Measure the diode voltage and circuit current as before, plotting the combination on the graph and confirming that each point is on a load line. You will start to see the diode's characteristic curve appear as the sequence of plotted points!

Return V_S to 3 V and change R_L to each of the following values, drawing a new load line at each step: 100, 220, 470, 1000, 2.2 k, and 4.7 kΩ. Measure and plot V_F and I_F at each step. This will fill in even more points, each very close to the load line for that value of R_L. As you can see, if you had enough values of R_L and sufficient power supply range, you could determine the diode's characteristic curve exactly!

You'll also have noticed that while you were only varying V_S, the load lines were parallel, but when R_L was varied, the load line slopes changed. That's because the slope of the load line is $-1/R_L$. Lower load resistance results in a steeper load line.

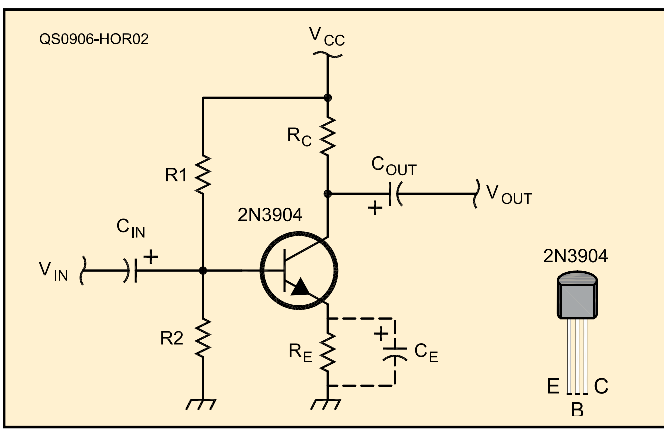

Figure 2 — The common-emitter (CE) amplifier uses a resistive voltage divider (R1 and R2) to establish the circuit's Q point along with R_E. The capacitor C_E is an emitter bypass capacitor that provides higher ac gain while leaving dc biasing unaffected.

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Transistor Amplifier Load Line

The load line is much more useful in designing transistor circuits, since current and voltage can take wide ranges of values. The common emitter (CE) amplifier in Figure 2, from the first Hands-On Radio experiment is one you'll use frequently, so we'll use it as an example.[2] This circuit uses self bias and emitter degeneration to establish a stable *Q point* (the operating point with no input signal).

The characteristic curves for a typical 2N3904 NPN transistor in the CE configuration are shown in Figure 3. Instead of just having a single characteristic curve as did the diode, a transistor's I_C–V_{CE} characteristic curve can change. As base current varies, the height of the curve changes on the graph. The set of curves show "snapshots" of the transistor's characteristic curve, each at a different value of base current.

Because the load for the circuit is resistive (consisting of R_C+R_E), the operating point falls along the dc load line drawn on the characteristic curves. We'll get to the ac load line later. As with the diode circuit, the intersection of the load line with the characteristic curve corresponding to the value of base current is the circuit's operating point. If you imagine one of the constant base current lines moving up and down as an input signal varies the base current, you can see its intersection with the load line moving, too. When no signal is applied, the base current is fixed at the level of bias current chosen by the designer and that operating point is the circuit's Q point. In the case of our CE amplifier, the values of R_1, R_2 and R_E determine the location of the Q point by controlling the value of the base bias current.

V_{CC} and the values of R_C and R_E determine the orientation of the load line. The two end points of the load line correspond to transistor saturation [$I_{Csat} = V_{CC} / (R_C+R_E)$ on the I_C axis] and cutoff (V_{CC} on the V_{CE} axis). The slope of the load line is $-1/(R_C+R_E)$, because the output current of the transistor flows through both the collector and emitter resistors.

In order to experiment with the load line, here are a set of components that will result in a Q point of I_{CQ} = 4 mA, V_{CEQ} = 5 V and a voltage gain of –5 with V_{CC} = +12 V: R_E = 270 Ω, R1 = 39 kΩ, R2 = 6.8 kΩ, and RC = 1.5 kΩ. (10 µF capacitors will be fine for C_{IN} and C_{OUT}.) Download and print the sample 2N3904 characteristic curves from the Hands-On Radio Web site and draw the load line between cutoff and saturation in this circuit. (The Q point should be on the load line.)

Build the circuit and verify that the values of I_{CQ} and V_{CEQ} are about right. Apply a 1 kHz, 0.5 V_{P-P} sine wave at the input and verify that the output signal is about five times larger and inverted from the input. Increase the input voltage until the output waveform becomes clipped at either the top or bottom and then reduce the input voltage by about half.

Now move the Q point by changing the value of I_{BQ}. To do this without changing the load line, adjust the ratio of R1 and R2 to change V_B, keeping the sum of the resistors in the range of 20 k to 50 kΩ. (You can substitute a 50 kΩ potentiometer for R1 and R2, with the wiper connected to the transistor base.) Measure the new values of I_{CQ} and V_{CEQ}, locate the new Q point on the load line, and observe the effect on the output waveform. For example, doubling the value of R2 will raise the value of I_{BQ} dramatically and probably cause the output waveform to be clipped at the bottom. This is because the higher bias current has moved the Q point farther along the load line toward saturation (left), making it easier for an input signal to drive V_{CE} lower into the saturation region.

[2]Previous Hands-On Radio columns and a complete parts list for all experiments are available to ARRL members at **www.arrl.org/tis/info/HTML/Hands-On-Radio** and in Experiment #76 (see next note).

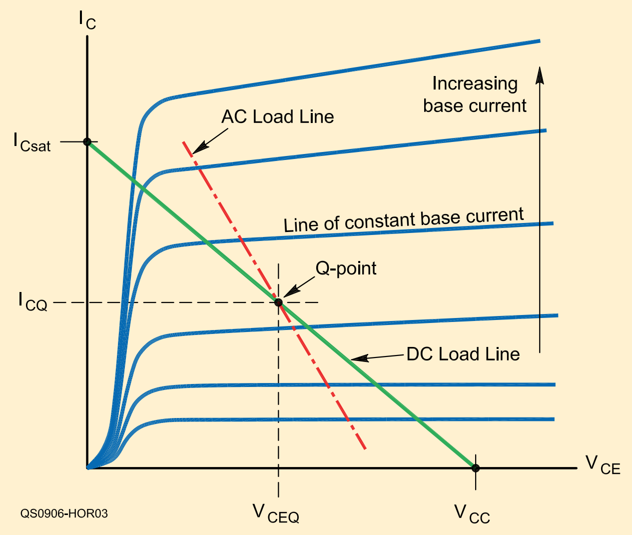

Figure 3 — The dc load line's end points correspond to transistor saturation (I_{Csat}) and cutoff (V_{CC}). The circuit operates somewhere on the load line depending on bias. The operating point with no signal applied is the quiescent, or Q point. By adding an emitter bypass capacitor, there is less load impedance for an ac signal, increasing the slope of the ac load line.

AC Load Lines

Figure 2 shows an *emitter bypass* capacitor, C_E, next to R_E. When C_E is connected across R_E, the circuit has a different ac voltage gain $A_V = -R_C/r_e$ (r_e is the internal emitter resistance of a few ohms) than dc gain $A_V = -R_C/R_E$. For an ac signal, the circuit operates on a separate ac load line as shown in Figure 3, because R_E has been effectively short circuited for ac signals. Without R_E, the slope of the ac load line is $-1/R_C$, steeper than for the dc load line. The ac and dc load lines intersect at the circuit's Q point because the circuit's ac and dc operation is the same if the ac input signal is zero.

Parts List[3]

- 1N4001 diode
- 2N3904 transistor
- 100, 220, 270, 470, 1000, 1.5 k, 2.2 k, 4.7 k, 6.8 k and 39 kΩ, ¼ W resistors
- 3 each 10 µF, 25 V electrolytic capacitors

Recommended Reading

Even for non-engineers, used copies of first- and second-year circuit engineering textbooks make fine workbench references for all sorts of circuit questions. Two of my favorites are Hayt and Kemmerly's *Engineering Circuit Analysis* and Millen and Grabel's *Microelectronics*, both published by McGraw-Hill. The former is good for basic R-L-C circuit mechanics and the latter for semiconductor circuits.

Next Month

You've heard terms before such as "SWR bridge," "noise bridge," "Wheatstone bridge" and so forth. We'll cross that bridge next month as we take a look at bridge circuits and why they are so useful.

[3]A parts kit for the first 61 experiments is available from your ARRL dealer or the ARRL Bookstore, ARRL order no. 1255K. Telephone 860-594-0355, or toll-free in the US 888-277-5289; **www.arrl.org/shop/**; **pubsales@arrl.org**.

Strays

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Title: Experiment #3--Basic Operational Amplifiers
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Experiment #3—Basic Operational Amplifiers

Let's give transistors a rest this month and take a look at one of the most popular components in electronics—the op-amp. The most widely used circuits are two simple amplifiers and an adder circuit.

Background

Op-amp is an abbreviation for *operational amplifier*, a term coined 70 years ago. Complicated mathematical equations were then solved by analog computers. Amplifiers were used to add, multiply, integrate, or perform other "operations" on signals. Originally made with vacuum tubes, integrated circuit op amps—such as the 741—started a revolution in electronics.

Op-amps generally have a high voltage gain, a high input impedance and a low output impedance. These properties make designing op-amp circuits easy because they simplify the design equations, as we'll see.

Terms to Learn

Inverting (–) and non-inverting (+)—signals at the inverting input cause the op-amp output to respond in the opposite "direction" and, for signals at the non-inverting input, in the same direction.

Negative feedback—routing some of a circuit's output back to the input in such a way as to oppose the effect of the input signal.

The Operational Amplifier

Figure 1 shows the basic op-amp symbol, including the inverting and non-inverting inputs. *The 2003 ARRL Handbook* incorrectly shows the pin-outs for several popular op-amps on page 24.27—the inverting and non-inverting input connections are *reversed.* The industry standard for single op-amp ICs is that pin 2 is the inverting input (–) and pin 3 the non-inverting input (+).

The bypass or decoupling capacitors (C1, C2) shown in Figure 1 keep the power bus clean and help prevent feedback paths that might cause the op-amp circuit to oscillate. They bypass the power connections to ground, hence "decoupling" ac signals from the circuit.

An op-amp has a huge capacity to amplify—80 dB or more of voltage gain at dc! Most of the time that's far too much gain, but so-called "negative feedback" can control that gain, creating useful behavior. Consider that the op-amp's gain is acting solely on the voltage differential between its two inputs. The trick is to connect components from the output to the inputs so that when the output is doing what we want, the voltages at both input pins are balanced. This is a "correction" or "feedback" signal. It stabilizes the op-amp output by correcting its input. If the input changes—even a little bit—the high gain immediately causes the op-amp to react, changing its output and the feedback signal until its inputs are balanced once again. When feedback is used we refer to the circuit being "closed-loop."

The Non-Inverting Amplifier

Figure 2A shows a non-inverting amplifier. The input signal, V_I, is connected directly to the non-inverting (+) input, while resistors R_f and R form a feedback network. Remember that the op-amp has a very high input impedance, so we can

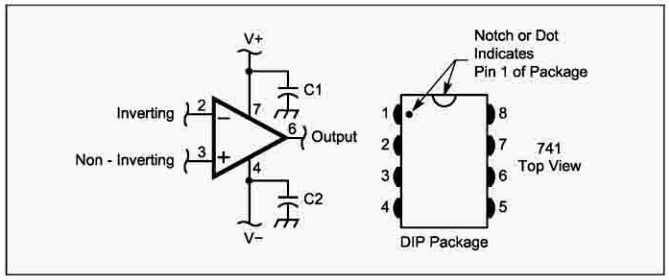

Figure 1—The operational-amplifier schematic symbol and typical package details.

treat the series combination of R and R_f as a voltage divider connected between the output pin and ground. The voltage at the inverting (–) input of the op-amp, V_i, must be:

$$V_i = V_{out} R / (R + R_f)$$

Since the op-amp's inputs must balance, $V_i = V_I$ and the circuit's gain, A_v must be:

$$A_v = V_{out} / V_I = (R + R_f) / R = 1 + R_f / R \quad [1]$$

The non-inverting amplifier's gain is always greater than 1 and is determined only by the ratio of R_f and R. There's no magic—the op-amp is just connected so that when its output is the correct amount larger than the input signal, both inputs balance.

Testing the Non-Inverting Amplifier

• Design the amplifier to have a gain of 2. That requires R_f = R. Use a value of 1 kΩ for this first circuit. Your power supply should be set to at least ±12 V (+12 V if you are using a single-polarity supply). Caution—do not apply signals above or below the power supply to the op-amp inputs or you may damage the IC.

• Build the circuit as shown in Figure 2A, including a 10 µF bypass capacitor to ground at each power supply pin. The 1 kΩ potentiometer will serve as an adjustable voltage source for V_I. Set the potentiometer so that the resistance from the wiper to ground is about 100 Ω. After checking all your connections, apply power and measure V_I and V_{out}. V_I should be approximately 1.2 V (one-tenth of V+) and V_{out} should be close to twice the value of V_I.

• The voltage at the inverting input, V_i should follow V_I very closely.

• Adjust the potentiometer output voltage up and down while measuring both V_I and V_{out}.

• You need a ±12 V power supply for this step. Replace the potentiometer with a function generator supplying a 1 V_{p-p}, 1 kHz sine wave. Use the oscilloscope to measure the output—it should be just like the input, but with twice the voltage.

• Experiment by changing the ratio of R and R_f to obtain different gains. (Keep resistor values above 100Ω.)

• Make a unity-gain voltage follower by removing R and replacing R_f with a direct connection as shown in Figure 2B. This circuit is frequently used to isolate a sensitive input or drive a heavy load.

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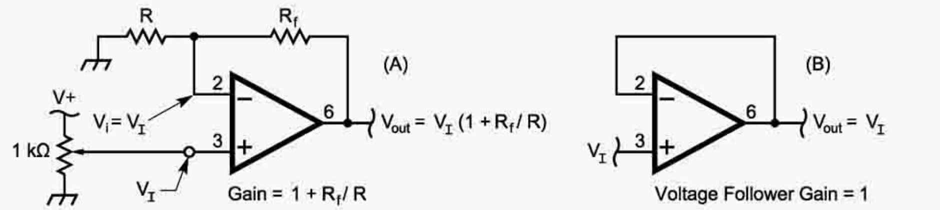

Figure 2—The non-inverting amplifier and a voltage follower.

The Inverting Amplifier

The high-impedance of the op-amp input can be used to create an inverting amplifier whose gain is also set by the ratio of two resistors. In Figure 3, R and R_f are again connected to the inverting input, but the input signal is connected to the free end of R and the non-inverting input is grounded. How does this work? Remember that the op-amp inputs are balanced, so the inverting input must also be at ground potential. It's not grounded, it's just at ground potential. This is called a "virtual ground."

With the inverting input at 0 V, the current through R must be $I_I = V_I / R$. Remember, too, that the op-amp input impedance is very high, so the input current must be balanced by the op-amp's output removing just as much current through Rf as flows through R. By Ohm's Law, the output voltage is then:

$$V_{out} = 0 - (I_I)\, R_f = -(V_I / R)\, R_f = -V_I R_f / R$$

and the gain must be:

$$A_v = V_{out} / V_I = -(V_I R_f / R)/V_I = -R_f / R \quad [2]$$

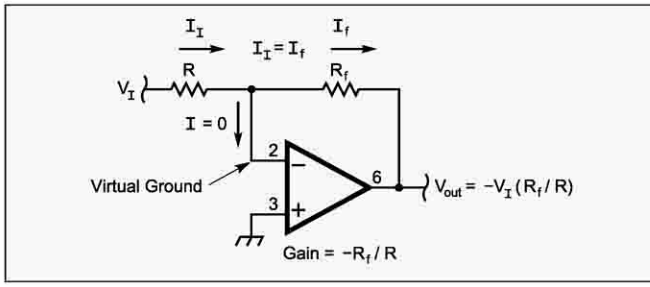

Figure 3—The inverting amplifier.

Testing the Inverting Amplifier

• Design the amplifier to have a gain of –4. Select a value for R of 1 kΩ. This requires R_f to be 4 kΩ. The closest standard value is 3.9 kΩ. You will need a ±12 V power supply to test this amplifier configuration.

• Build the amplifier as shown in Figure 3 and connect a 1 V_{p-p}, 1 kHz sine wave to the input. You should see a 3.9 V_{p-p} sine wave at the output, but inverted with respect to the input. Look at the inverting input to verify that it is at ground potential.

• Use different resistor ratios to change the gain. (Keep resistor values above 100 Ω to limit how much power the op-amp must supply.) Input a dc voltage by using the 1 kΩ potentiometer as before and see if the circuit output is of the opposite polarity.

The Summing Amplifier

The circuit of Figure 4 shows how more than one signal can be combined and amplified by a summing amplifier. As for the inverting amplifier, the op-amp must balance all of the currents at the inverting input—even if current comes from more than one source!

The current from each input signal equals V_{in} / R, so the total current in R_f must be their sum:

$$I_f = V_{in1} / R_1 + V_{in2} / R_2$$

Using the same reasoning as before, the output voltage must be:

$$V_{out} = -(V_{in1} / R_1 + V_{in2} / R_2)R_f \quad [3]$$

The gain for either input signal is still the ratio, $-R_f / R$.

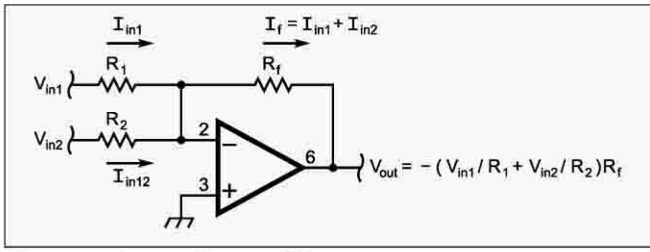

Figure 4—A summing amplifier.

Testing the Summing Amplifier

• Design the amplifier to have a gain of –1 for each input by setting all three resistors (R_1, R_2 and R_f) to 10 kΩ. You will need a ±12 V power supply to test this amplifier configuration.

• Build the circuit and input the 1 V_{p-p}, 1 kHz sine wave to input 1. Use the 1 kΩ potentiometer as before to supply input 2.

• Vary the potentiometer while watching the output on your oscilloscope. You will see the inverted sine wave from input 1 shifted up and down as the dc level at input 2 changes.

• Experiment by altering the ratio of either input resistor and R_f to observe the effect on the addition of signals. Replace R_1 or R_2 (or both) with a 10 kΩ potentiometer and vary the channel ratios independently. Congratulations—you've just built a 2-channel mixer!

Suggested Reading

The 2003 ARRL Handbook, pp 8.32-8.35; Horowitz and Hill, *The Art of Electronics*, chapter 4, sections 4.01-4.08; Ian Poole, G3YWX, "An Introduction to Op Amps," *QST*, Feb 1999, pp 55-56. The ARRL Web site for this series is **www.arrl.org/tis/info/html/hands-on-radio/**. Use it!

Shopping List

You'll need the following components:

• 741 op-amp—The part may be labeled as an LM741CN, MC1741CP1, µA741C, etc. The prefixes and suffixes identify the manufacturer, package style and temperature grade. RadioShack part number 276-007 will fill the bill.

• ¼ W resistors of the following values: 1 kΩ (2 ea), 3.9 kΩ, 10 kΩ (4 ea) and miscellaneous values between 1 kΩ and 10 kΩ.

• 1 kΩ and 10 kΩ potentiometer (single or multi-turn).

• 2—10 µF capacitors with a voltage rating of 25 V dc or more.

Next Month

Op-amps are frequently used as the engine driving an active filter. Sprinkle on a few capacitors and resistors and next month we'll see just how easy creating an audio filter can be.

Cathode Ray Tubes (CRT)

A variation of the vacuum tube that is widely used in oscilloscopes and television monitors is the *cathode ray tube (CRT)*, diagrammed in **Fig 1**. The CRT has a cathode and grid much like a triode tube. The plate, usually referred to as the *anode* in this device, is designed to accelerate the electrons to very high velocities, with anode voltages that can be as high as tens of thousands of volts. The anode of the CRT differs from the plates of other vacuum tubes, since it is designed as a set of plates that are parallel to the electron beam. The anode voltage accelerates the electrons but does not absorb them. The electron beam passes by the anode and continues to the face of the tube. The cathode, grid and anode are all located in the neck of the CRT and are collectively referred to as the *electron gun*.

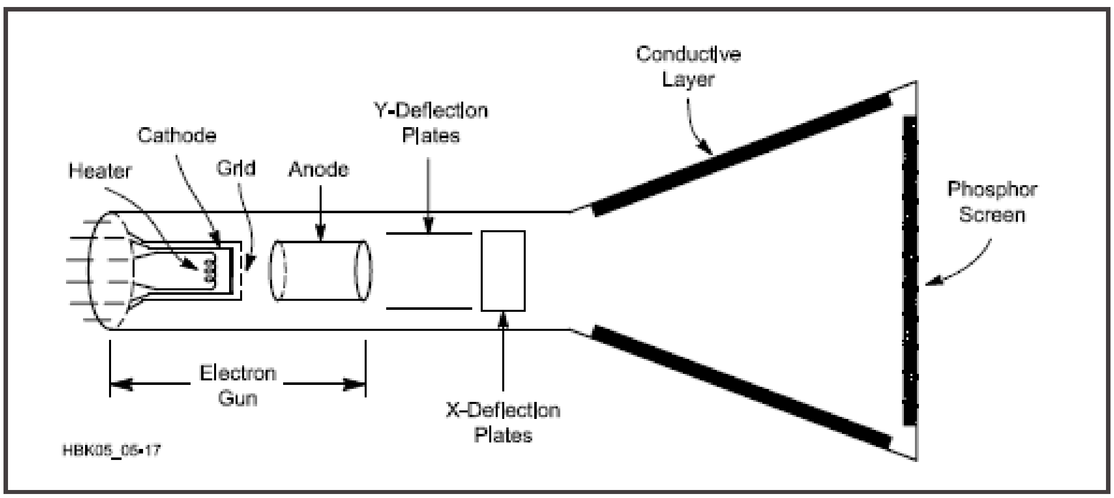

Fig 1 — Cross section of CRT. The electron gun generates a stream of electrons and is made up of a heater, cathode, grid and anode (plate). The electron beam passes by two pairs of deflection plates that deviate the path of the beam in the vertical (y) direction and then the horizontal (x) direction. The deflected electron beam strikes a phosphor screen and causes it to glow at that spot. Any electrons that bounce off the screen are absorbed by the conductive layer along the sides of the tube, preventing spurious luminescence.

The electron beam is deflected from its path by either magnetic deflectors that surround the yoke of the tube or by electrostatic deflection plates that are built into the tube neck just beyond the electron gun. A CRT typically has two sets of deflectors: vertical and horizontal. When a potential is applied to a set of deflectors, the passing electron beam is bent, altering its path. In an oscilloscope, the time base typically drives the horizontal deflectors and the input signal drives the vertical deflectors, although in many oscilloscopes it is possible to connect another input signal to the horizontal deflectors to obtain an X-Y, or vector, display. In televisions and some computer monitors the deflectors typically are driven by a raster generator. The horizontal deflectors are driven by a sawtooth pattern that causes the beam to move repeatedly from left to right and then retrace quickly to the left. The vertical deflectors are driven by a slower sawtooth pattern that causes the beam to move repeatedly from top to bottom and then retrace quickly to the top. The relative timing of the two sawtooth patterns is such that the beam scans from left to right, retraces to the left and then begins the next horizontal trace just below the previous one.

Beyond the deflectors, the CRT flares out. The front face is coated with a phosphorescent material that glows when struck by the electron beam. To prevent spurious phosphorescence, a conductive layer along the sides of the tube absorbs any electrons that reflect off the glass.

Vector displays have better resolution than raster scanning. The trace lines are clearer, which is the reason oscilloscope displays use this technique. It is faster to fill the screen using raster scanning, however. This is why TVs use raster scanning.

Some CRT tubes are designed with multiple electron beams. The beams are sometimes generated by different electron guns that are placed next to each other in the neck of the tube. They can also be generated by splitting the output of a single electron gun into two or more beams. Very high quality oscilloscopes use two electron beams to trace two input channels rather than the more common method of alternating a single beam between the two inputs. Color television tubes use three electron beams for the three primary colors (red, green and blue). Each beam is focused on only one of these colored phosphors, which are interleaved on the face of the tube. A metal shadow mask keeps the colors separate as the beams scan across the tube.